20MHz Bandwidth, Low Noise CMOS Op-amps

Features

- **Gain-bandwidth Product: 20MHz**
- **Low Noise: 7.3nV/√Hz(f= 1kHz)**
- **Slew Rate: 25 V/μs**
- **Offset Voltage: 1 mV (max)**
- **Low THD+N: 0.0005%**
- **Supply Range: 2.2V to 5.5V**
- **Supply Current: 3.5 mA/ch**
- **Low Input Bias Current: 0.3pA Typical**
- **Rail-to-Rail I/O**
- **High Output Current: 70mA (1.0V Drop)**
- **–40°C to 125°C Operation Range**
- **Robust 8kV – HBM and 2kV – CDM ESD Rating**

Applications

- Sensor Signal Conditioning
- Consumer Audio
- Multi-Pole Active Filters
- Control-Loop Amplifiers
- Communications
- Security
- Scanners

Description

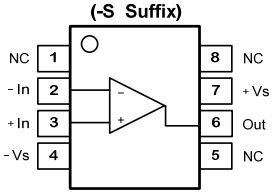
The TP240x series consists of single, dual, and quad-channel CMOS operational amplifiers featuring low noise and rail-to-rail inputs/outputs optimized for low-power, single-supply applications. Specified over a wide supply range of 2.2 V to 5.5 V, the low quiescent current of only 3.5 mA per channel makes these devices well-suited for power-sensitive applications.

The combination of very low noise (7.3 nV/√Hz at 1 kHz), high gain-bandwidth (20 MHz), and fast slew rate (25 V/μs) make the TP240x family ideal for a wide range of applications, including signal conditioning and sensor amplification requiring high gains. Featuring low THD+N, the TP240x series is also excellent for consumer audio applications, particularly for single-supply systems.

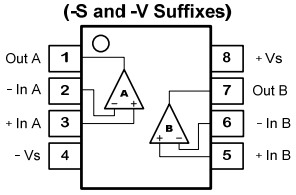
The TP2401 is single channel version available in 8-pin SOIC and 5-pin SOT23 packages. The TP2402 is dual channel version available in 8-pin SOIC and MSOP packages. The TP2404 is quad channel version available in 14-pin SOIC and TSSOP packages.

Pin Configuration (Top View)

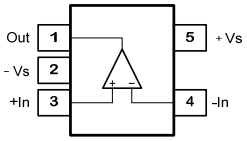
TP2401
8-Pin SOIC
(-S Suffix)



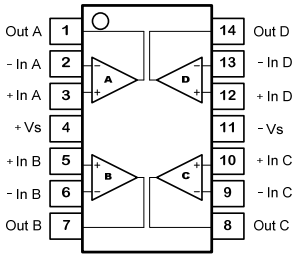
TP2402
8-Pin SOIC/MSOP
(-S and -V Suffixes)



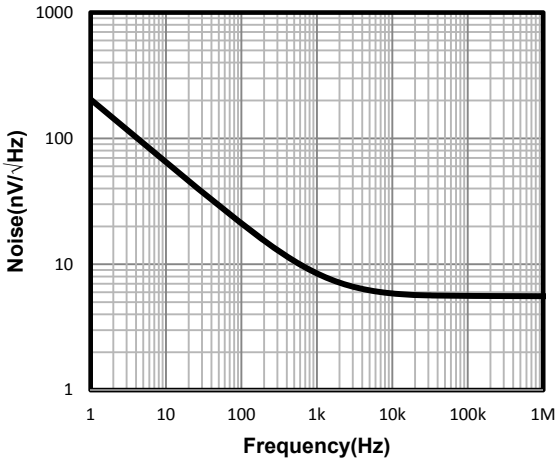
TP2401
5-Pin SOT23
(-T Suffix)



TP2404
14-Pin SOIC/TSSOP
(-S and -T Suffixes)



Input Voltage Noise Spectral Density



Order Information

Model Name	Order Number	Package	Transport Media, Quantity	Marking Information
TP2401	TP2401-SR	8-Pin SOIC	Tape and Reel, 4,000	TP2401
	TP2401-TR	5-Pin SOT23	Tape and Reel, 3,000	401
TP2402	TP2402-SR	8-Pin SOIC	Tape and Reel, 4,000	TP2402
	TP2402-VR	8-Pin MSOP	Tape and Reel, 3,000	TP2402
TP2404	TP2404-SR	14-Pin SOIC	Tape and Reel, 2,500	TP2404
	TP2404-TR	14-Pin TSSOP	Tape and Reel, 3,000	TP2404

Absolute Maximum Ratings Note 1

Supply Voltage: $V^+ – V^–$ Note 2 ..... 7.0V
Input Voltage..... $V^–$ – 0.3 to V^+ + 0.3
Input Current: +IN, –IN Note 3 ..... ±20mA
Output Current: OUT..... ±160mA
Output Short-Circuit Duration Note 4 ..... Infinite
Current at Supply Pins……..... ±60mA
Operating Temperature Range.....–40°C to 125°C
Maximum Junction Temperature..... 150°C
Storage Temperature Range..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 260°C

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The op amp supplies must be established simultaneously, with, or before, the application of any input signals.

Note 3: The inputs are protected by ESD protection diodes to each power supply. If the input extends more than 500mV beyond the power supply, the input current should be limited to less than 10mA.

Note 4: A heat sink may be required to keep the junction temperature below the absolute maximum. This depends on the power supply voltage and how many amplifiers are shorted. Thermal resistance varies with the amount of PC board metal connected to the package. The specified values are for short traces connected to the leads.

ESD, Electrostatic Discharge Protection

Symbol	Parameter	Condition	Minimum Level	Unit
HBM	Human Body Model ESD	MIL-STD-883H Method 3015.8	8	kV
CDM	Charged Device Model ESD	JEDEC-EIA/JESD22-C101E	2	kV

Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
5-Pin SOT23	250	81	°C/W
8-Pin SOIC	158	43	°C/W
8-Pin MSOP	210	45	°C/W
14-Pin SOIC	120	36	°C/W
14-Pin TSSOP	180	35	°C/W

Electrical Characteristics

The specifications are at T_A = 27°C. V_S = +2.2 V to +5.5 V, or ±1.1 V to ±2.75 V, R_L = 2kΩ, C_L =100pF.Unless otherwise noted.

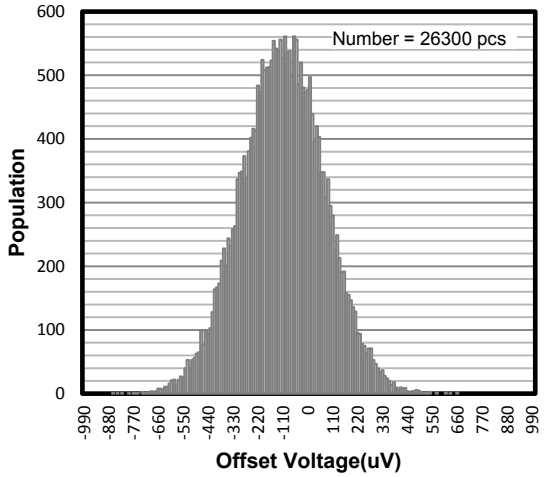
SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	V_{CM} = V_{DD}/2	-1	±0.3	+1	mV
V_{OS} TC	Input Offset Voltage Drift	-40°C to 125°C		1	2	µV/°C
I_B	Input Bias Current	T_A = 27 °C		0.3		pA
		T_A = 85 °C		150		pA
		T_A = 125 °C		300		pA
I_{OS}	Input Offset Current			0.001		pA
V_n	Input Voltage Noise	f = 0.1Hz to 10Hz		2.0		μV_{PP}
e_n	Input Voltage Noise Density	f = 1kHz		7.3		nV/√Hz
i_n	Input Current Noise	f = 1kHz		2		fA/√Hz
C_{IN}	Input Capacitance	Differential Common Mode		7.76 6.87		pF
CMRR	Common Mode Rejection Ratio	V_{CM} = 2V to 3V	80	100		dB
V_{CM}	Common-mode Input Voltage Range		V^- -0.3		V^+-0.3	V
PSRR	Power Supply Rejection Ratio	V_{CM} = 2.5V, V_S = 4V to 5V	80	100		dB
A_{VOL}	Open-Loop Large Signal Gain	R_{LOAD} = 2kΩ	100	130		dB
V_{OL}, V_{OH}	Output Swing from Supply Rail	R_{LOAD} = 2kΩ		13	20	mV
R_{OUT}	Closed-Loop Output Impedance	G = 1, f =1MHz, I_{OUT} = 0		0.043		Ω
R_O	Open-Loop Output Impedance	f = 1kHz, I_{OUT} = 0		125		Ω
I_{SC}	Output Short-Circuit Current	Sink or source current	110	130	200	mA
V_{DD}	Supply Voltage		2.2		5.5	V
I_Q	Quiescent Current per Amplifier	V_{DD} = 5V		3.5	5	mA
PM	Phase Margin	R_{LOAD} = 1kΩ, C_{LOAD} = 60pF		60		°
GM	Gain Margin	R_{LOAD} = 1kΩ, C_{LOAD} = 60pF		11		dB
GBWP	Gain-Bandwidth Product	f = 1kHz		20		MHz
SR	Slew Rate	AV = 1, V_{OUT} = 1.5V to 3.5V, C_{LOAD} = 60pF, R_{LOAD} = 1kΩ	18	25		V/µs
FPBW	Full Power Bandwidth Note 1			5.21		MHz
t_S	Settling Time, 0.1% Settling Time, 0.01%	AV = –1, 1V Step		0.29 0.45		µs
THD+N	Total Harmonic Distortion and Noise	f = 1kHz, AV =1, RL = 2kΩ, VOUT = 1Vp-p		123		dB
X_{talk}	Channel Separation	f = 1kHz, R_L = 2kΩ		110		dB

Note 1: Full power bandwidth is calculated from the slew rate FPBW = SR/π • V_{P-P}

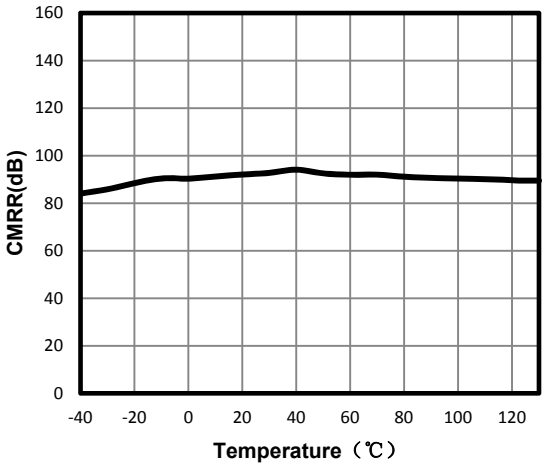
Typical Performance Characteristics

V_S = ±2.5V, V_{CM} = 0V, R_L = Open, unless otherwise specified.

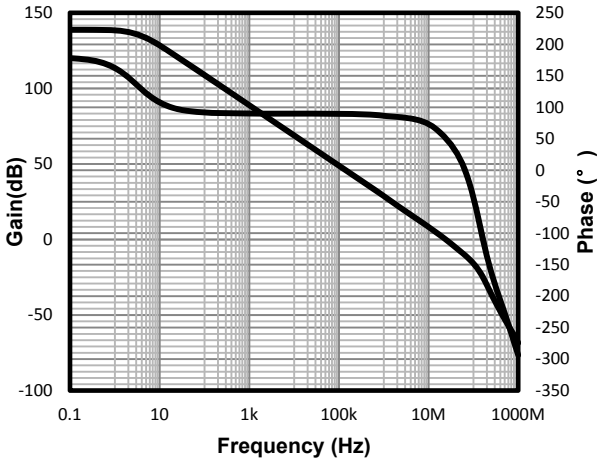
Offset Voltage Production Distribution



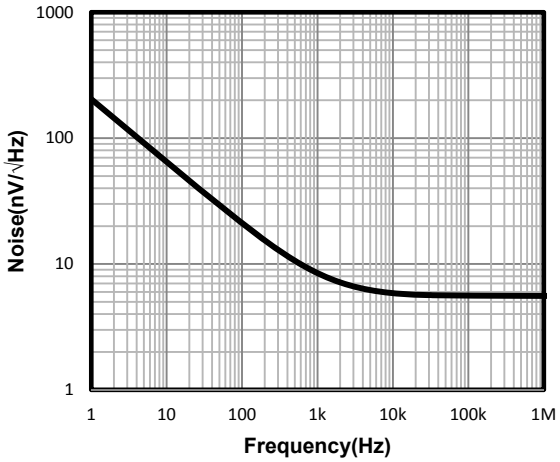
CMRR vs. Temperature



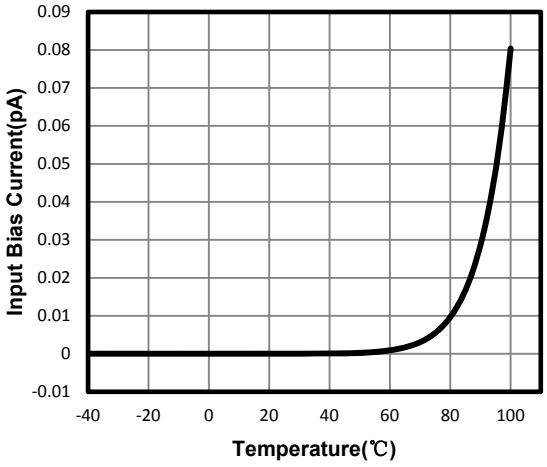
Open-Loop Gain and Phase



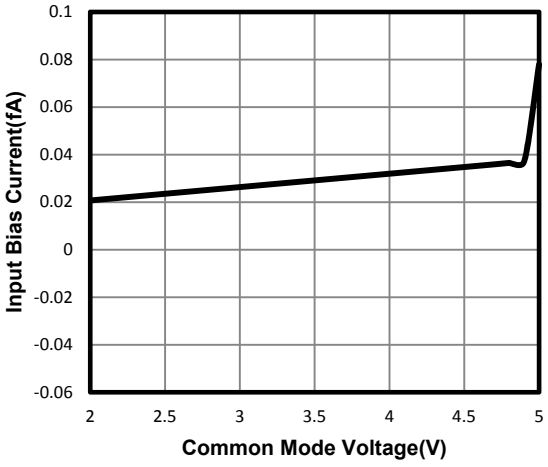
Input Voltage Noise Spectral Density



Input Bias Current vs. Temperature



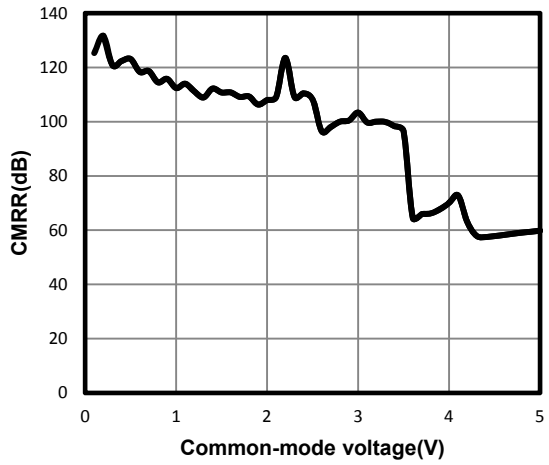
Input Bias Current vs. Input Common Mode Voltage



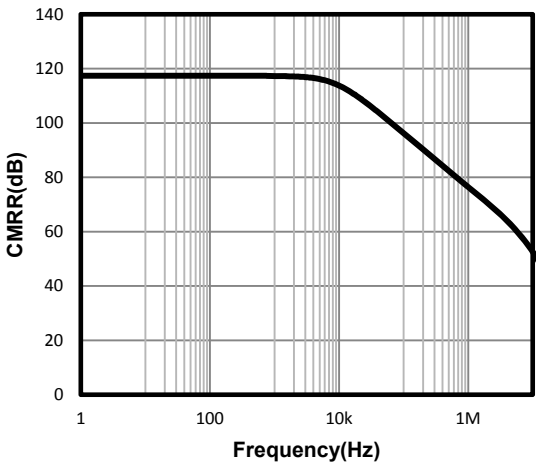
Typical Performance Characteristics

V_S = ±2.5V, V_{CM} = 0V, R_L = Open, unless otherwise specified. (Continued)

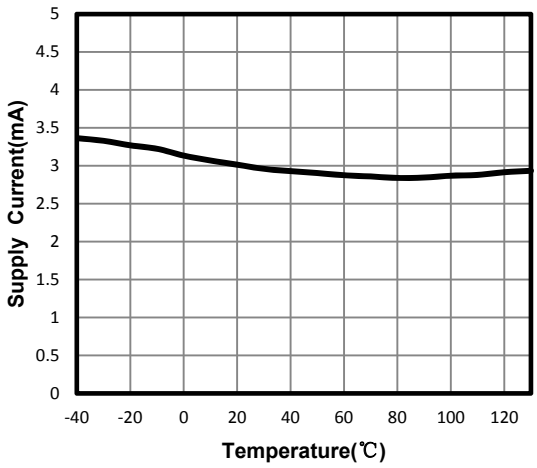
Common Mode Rejection Ratio



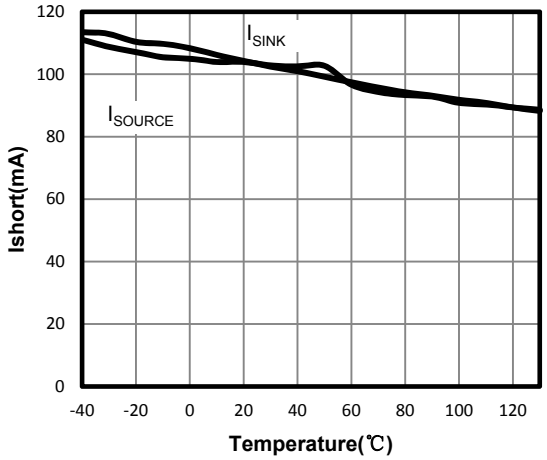
CMRR vs. Frequency



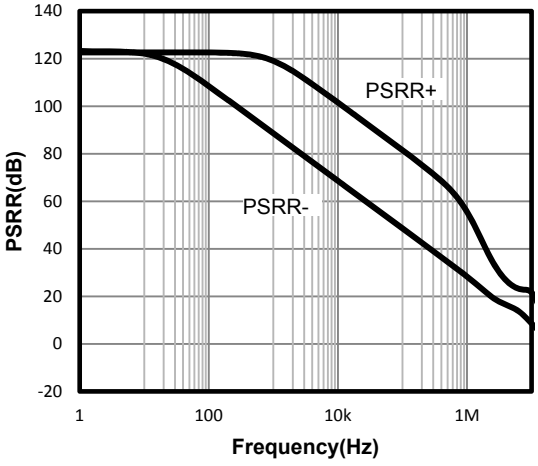
Quiescent Current vs. Temperature



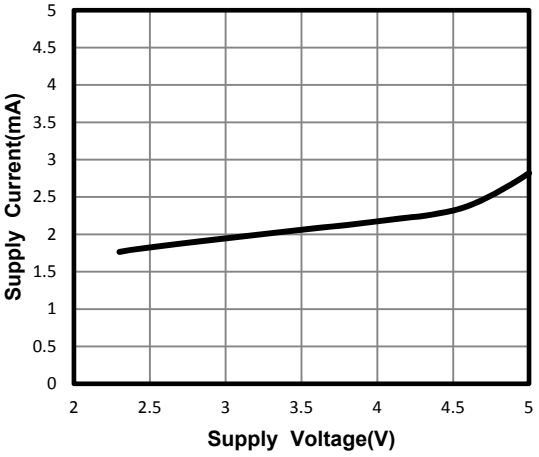
Short Circuit Current vs. Temperature



Power-Supply Rejection Ratio



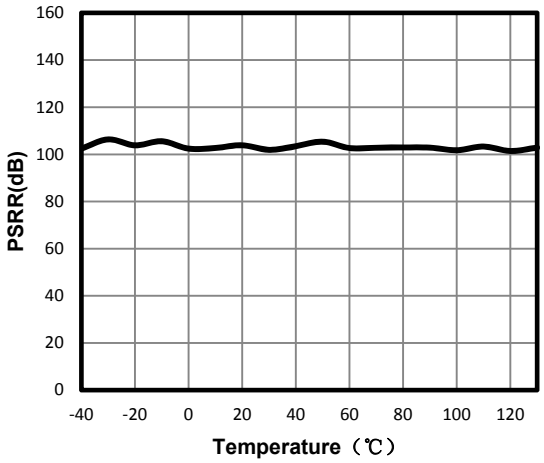
Quiescent Current vs. Supply Voltage



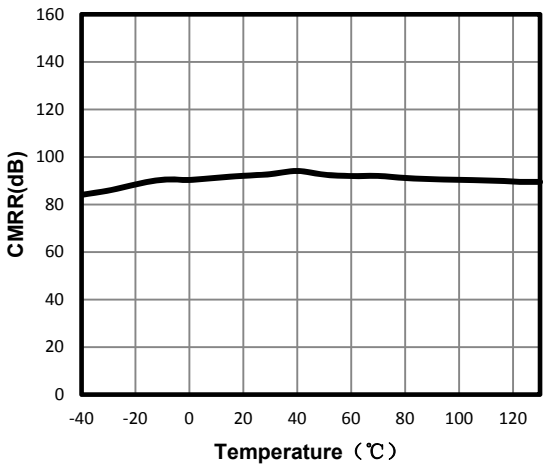
Typical Performance Characteristics

V_S = ±2.5V, V_{CM} = 0V, R_L = Open, unless otherwise specified. (Continued)

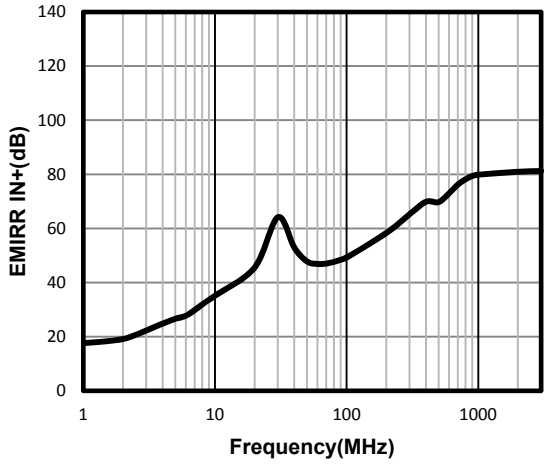
Power-Supply Rejection Ratio vs. Temperature



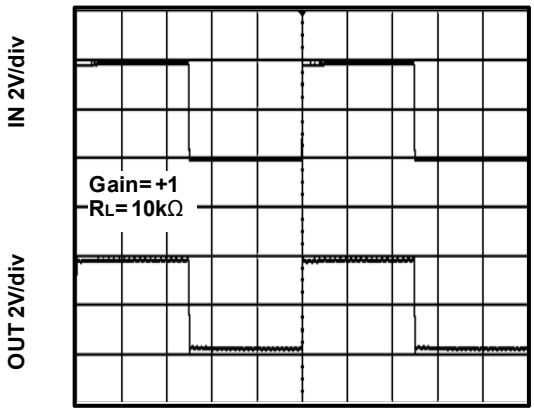
CMRR vs. Temperature



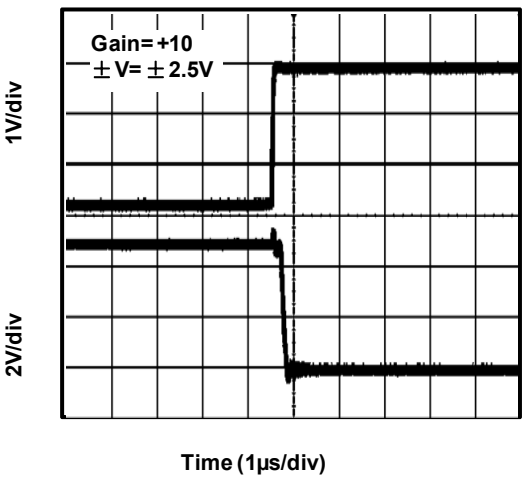
EMIRR IN+ vs. Frequency



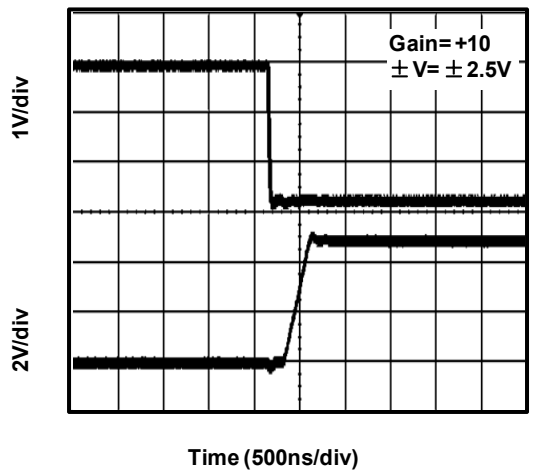
Large-Scale Step Response



Negative Over-Voltage Recovery



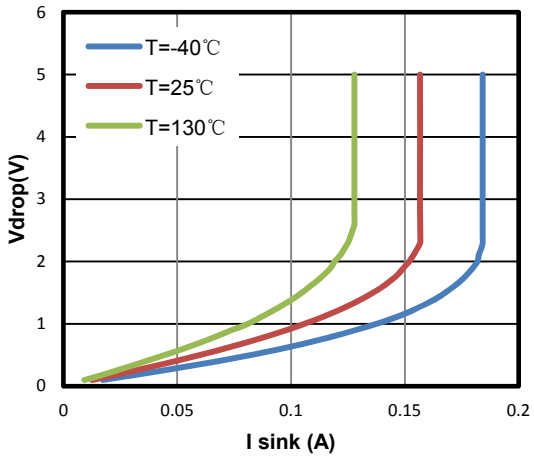
Positive Over-Voltage Recovery



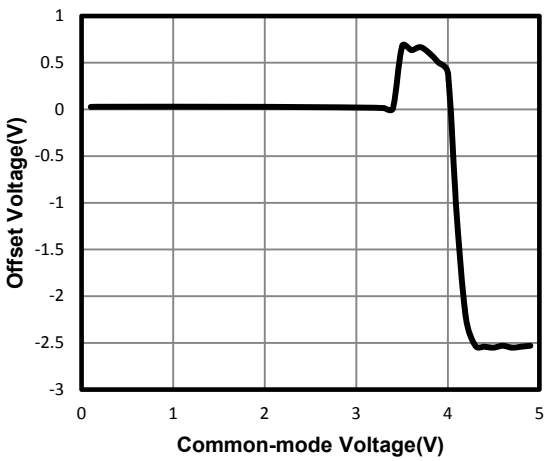
Typical Performance Characteristics

V_S = ±2.5V, V_{CM} = 0V, R_L = Open, unless otherwise specified. (Continued)

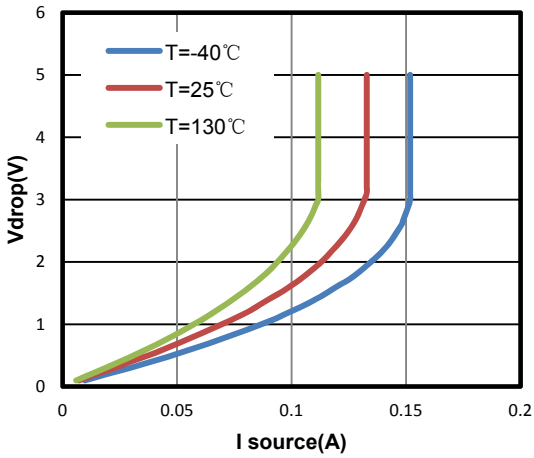
Negative Output Swing vs. Load Current



Offset Voltage vs Common-Mode Voltage



Positive Output Swing vs. Load Current



Pin Functions

-IN: Inverting Input of the Amplifier.

+IN: Non-Inverting Input of Amplifier.

OUT: Amplifier Output. The voltage range extends to within mV of each supply rail.

V+ or +Vs: Positive Power Supply. Typically the voltage is from 2.2V to 5.5V. Split supplies are possible as long as the voltage between V+ and V– is between 2.2V and 5.5V. A bypass capacitor of 0.1μF as close to the part as possible should be used between power supply pins or between supply pins and ground.

V- or -Vs: Negative Power Supply. It is normally tied to ground. It can also be tied to a voltage other than ground as long as the voltage between V_+ and V_- is from 2.2V to 5.5V. If it is not connected to ground, bypass it with a capacitor of 0.1μF as close to the part as possible.

Operation

The TP2401 series op amps can operate on a single-supply voltage (2.2 V to 5.5 V), or a split-supply voltage (±1.1 V to ±2.75 V), making them highly versatile and easy to use. The power-supply pins should have local bypass ceramic capacitors (typically 0.001 μF to 0.1 μF). These amplifiers are fully specified from +2.2 V to +5.5 V and over the extended temperature range of –40°C to +125°C. Parameters that can exhibit variance with regard to operating voltage or temperature are presented in the Typical Characteristics

Applications Information

Input ESD Diode Protection

The TP2401 incorporates internal electrostatic discharge (ESD) protection circuits on all pins. In the case of input and output pins, this protection primarily consists of current-steering diodes connected between the input and power-supply pins. These ESD protection diodes also provide in-circuit input overdrive protection, as long as the current is limited to 10 mA as stated in the Absolute Maximum Ratings table. Many input signals are inherently current-limited to less than 10 mA; therefore, a limiting resistor is not required. Figure 1 shows how a series input resistor (RS) may be added to the driven input to limit the input current. The added resistor contributes thermal noise at the amplifier input and the value should be kept to the minimum in noise-sensitive applications.

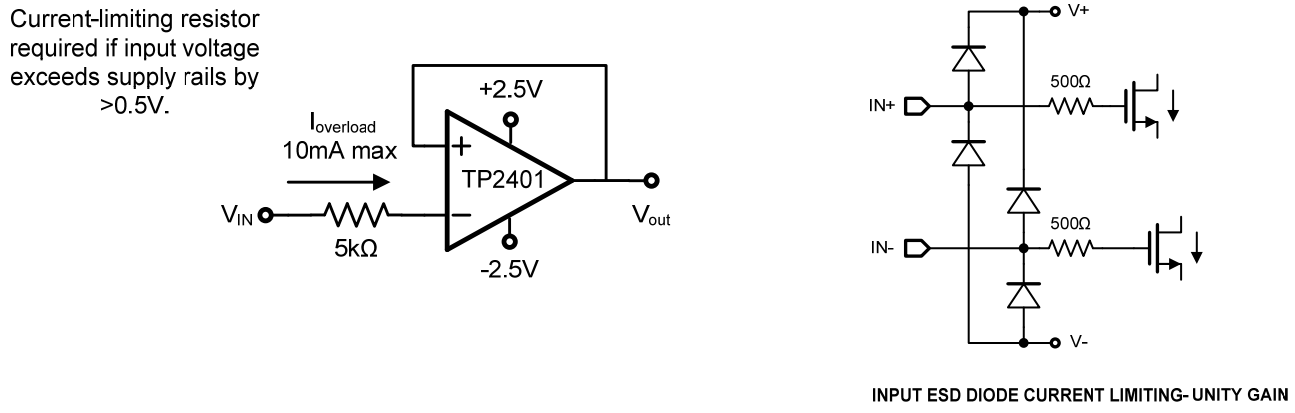


Figure1. Input ESD Diode

PHASE REVERSAL

The TP2401 op amps are designed to be immune to phase reversal when the input pins exceed the supply voltages, therefore providing further in-system stability and predictability. Figure 2 shows the input voltage exceeding the supply voltage without any phase reversal.

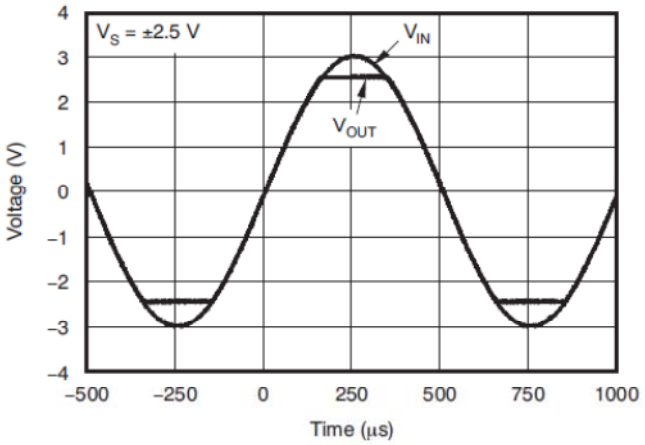


Figure 2. No Phase Reversal

EMI SUSCEPTIBILITY AND INPUT FILTERING

Operational amplifiers vary in susceptibility to electromagnetic interference (EMI). If conducted EMI enters the device, the dc offset observed at the amplifier output may shift from the nominal value while EMI is present. This shift is a result of signal rectification associated with the internal semiconductor junctions. While all operational amplifier pin functions can be affected by EMI, the input pins are likely to be the most susceptible. The TP2401 operational amplifier family incorporates an internal input low-pass filter that reduces the amplifier response to EMI. Both common-mode and differential mode filtering are provided by the input filter. The filter is designed for a cutoff frequency of approximately 400 MHz (–3 dB), with a roll-off of 20 dB per decade.

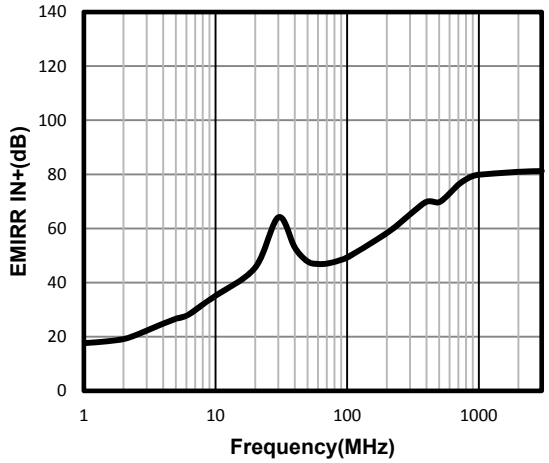


Figure 3. TP2401 EMIRR IN+ vs Frequency

ACTIVE FILTER

The TP2401 is well-suited for active filter applications that require a wide bandwidth, fast slew rate, low-noise, single-supply operational amplifier. Figure 4 shows a 20-kHz, second-order, low-pass filter using the multiplefeedback (MFB) topology. The components have been selected to provide a maximally-flat Butterworth response. Beyond the cutoff frequency, roll-off is –40 dB/dec. The Butterworth response is ideal for applications that require predictable gain characteristics, such as the anti-aliasing filter used in front of an ADC.

One point to observe when considering the MFB filter is that the output is inverted, relative to the input. If this inversion is not required, or not desired, a noninverting output can be achieved through one of these options:

1. adding an inverting amplifier;
2. adding an additional second-order MFB stage

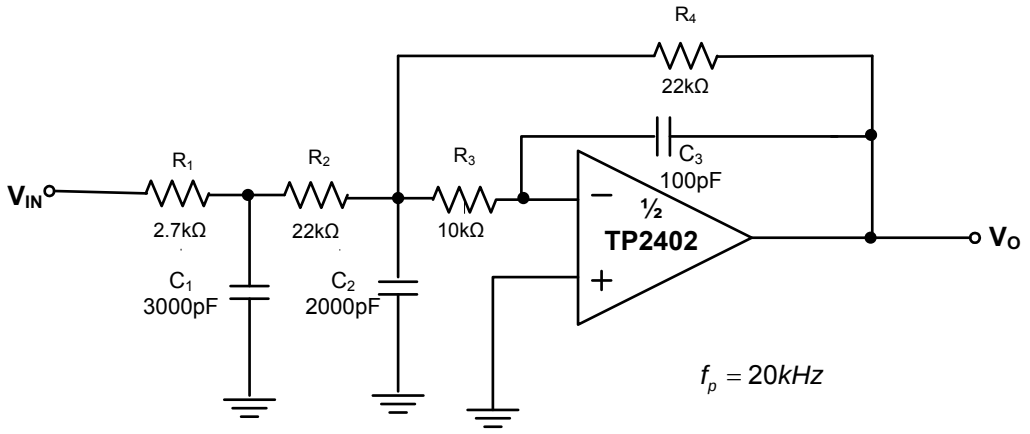


Figure 4. TP2402 Configured as a Three-Pole, 20-kHz, Sallen-Key Filter

PCB Surface Leakage

In applications where low input bias current is critical, Printed Circuit Board (PCB) surface leakage effects need to be considered. Surface leakage is caused by humidity, dust or other contamination on the board. Under low humidity conditions, a typical resistance between nearby traces is $10^{12}\Omega$. A 5V difference would cause 5pA of current to flow, which is greater than the TP2401/2402/2404 OPA's input bias current at +27°C (±3pA, typical). It is recommended to use multi-layer PCB layout and route the OPA's -IN and +IN signal under the PCB surface.

The effective way to reduce surface leakage is to use a guard ring around sensitive pins (or traces). The guard ring is biased at the same voltage as the sensitive pin. An example of this type of layout is shown in Figure 1 for Inverting Gain application.

1. For Non-Inverting Gain and Unity-Gain Buffer:
   a) Connect the non-inverting pin (V_{IN}+) to the input with a wire that does not touch the PCB surface.
   b) Connect the guard ring to the inverting input pin (V_{IN}–). This biases the guard ring to the Common Mode input voltage.
2. For Inverting Gain and Trans-impedance Gain Amplifiers (convert current to voltage, such as photo detectors):
   a) Connect the guard ring to the non-inverting input pin (V_{IN}+). This biases the guard ring to the same reference voltage as the op-amp (e.g., V_{DD}/2 or ground).
   b) Connect the inverting pin (V_{IN}–) to the input with a wire that does not touch the PCB surface.

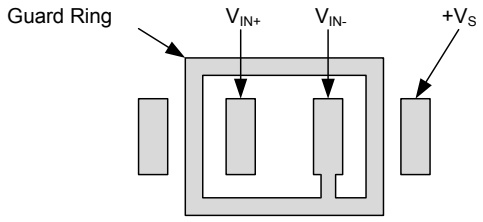


Figure 5 The Layout of Guard Ring

Power Supply Layout and Bypass

The TP2401/2402/2402 OPA's power supply pin (V_{DD} for single-supply) should have a local bypass capacitor (i.e., 0.01μF to 0.1μF) within 2mm for good high frequency performance. It can also use a bulk capacitor (i.e., 1μF or larger) within 100mm to provide large, slow currents. This bulk capacitor can be shared with other analog parts.

Ground layout improves performance by decreasing the amount of stray capacitance and noise at the OPA's inputs and outputs. To decrease stray capacitance, minimize PC board lengths and resistor leads, and place external components as close to the op amps' pins as possible.

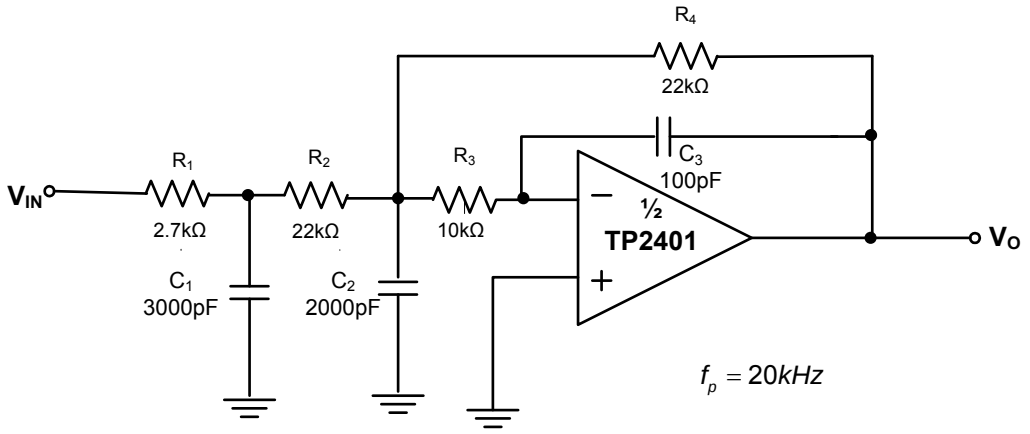
Proper Board Layout

To ensure optimum performance at the PCB level, care must be taken in the design of the board layout. To avoid leakage currents, the surface of the board should be kept clean and free of moisture. Coating the surface creates a barrier to moisture accumulation and helps reduce parasitic resistance on the board.

Keeping supply traces short and properly bypassing the power supplies minimizes power supply disturbances due to output current variation, such as when driving an ac signal into a heavy load. Bypass capacitors should be connected as closely as possible to the device supply pins. Stray capacitances are a concern at the outputs and the inputs of the amplifier. It is recommended that signal traces be kept at least 5mm from supply lines to minimize coupling.

A variation in temperature across the PCB can cause a mismatch in the Seebeck voltages at solder joints and other points where dissimilar metals are in contact, resulting in thermal voltage errors. To minimize these thermocouple effects, orient resistors so heat sources warm both ends equally. Input signal paths should contain matching numbers and types of components, where possible to match the number and type of thermocouple junctions. For example, dummy components such as zero value resistors can be used to match real resistors in the opposite input path. Matching components should be located in close proximity and should be oriented in the same manner. Ensure leads are of equal length so that thermal conduction is in equilibrium. Keep heat sources on the PCB as far away from amplifier input circuitry as is practical.

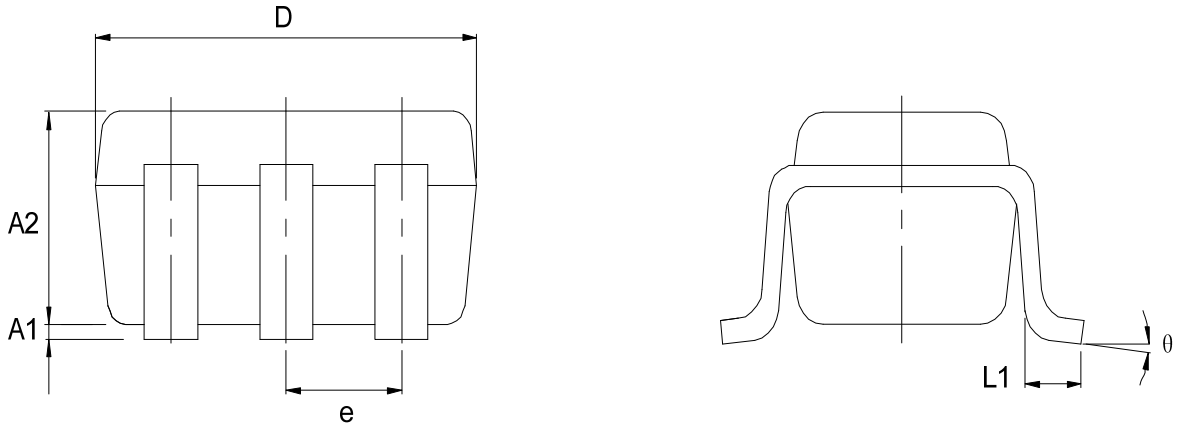
The use of a ground plane is highly recommended. A ground plane reduces EMI noise and also helps to maintain a constant temperature across the circuit board.

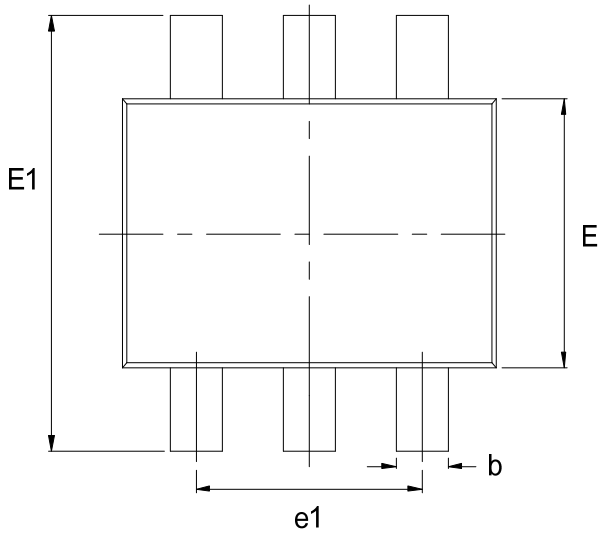


Three-Pole Low-Pass Filter

Package Outline Dimensions

SOT23-5

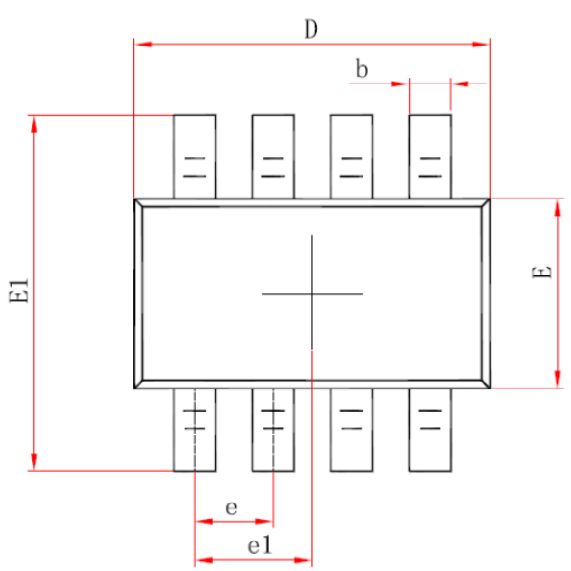


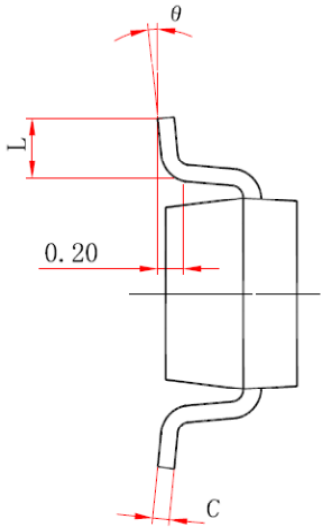


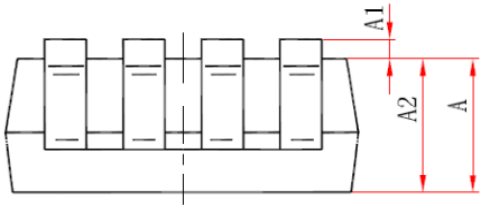
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.400	0.012	0.016
D	2.820	3.020	0.111	0.119
E	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.950TYP		0.037TYP	
e1	1.800	2.000	0.071	0.079
L1	0.300	0.460	0.012	0.024
θ	0°	8°	0°	8°

Package Outline Dimensions

SOT-23-8



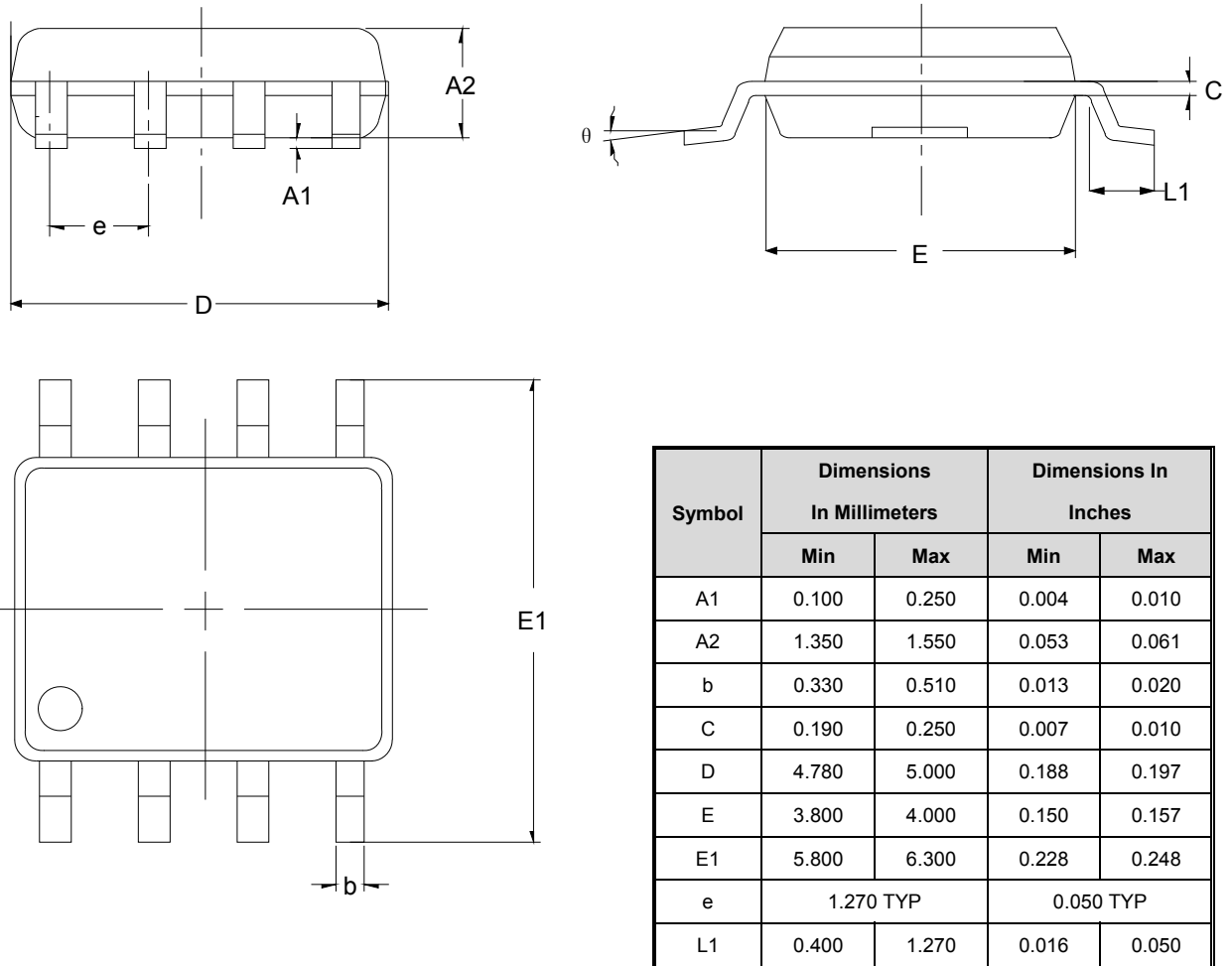




Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E	1.500	1.700	0.059	0.067
e	0.65（BSC）		0.026(BSC)	
e1	0.975（BSC）		0.038(BSC)	
L	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°

Package Outline Dimensions

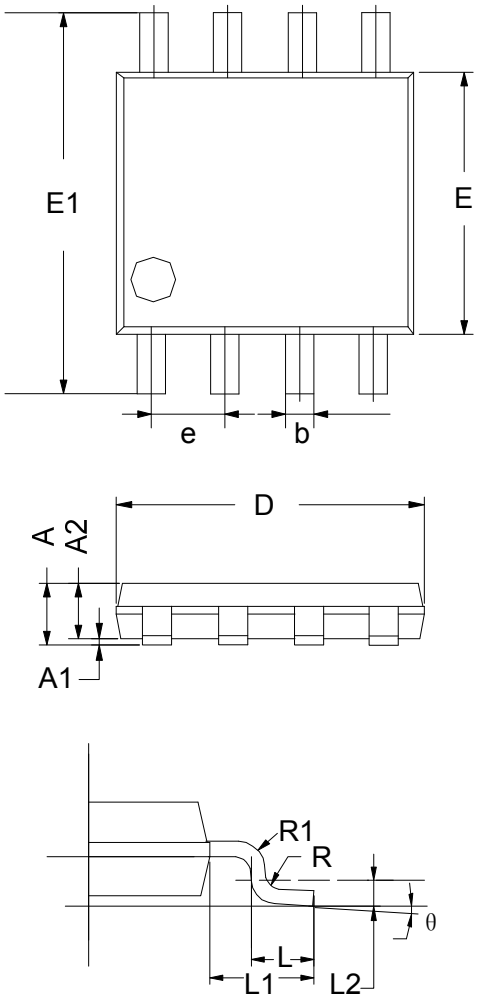
SO-8 (SOIC-8)



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
C	0.190	0.250	0.007	0.010
D	4.780	5.000	0.188	0.197
E	3.800	4.000	0.150	0.157
E1	5.800	6.300	0.228	0.248
e	1.270 TYP		0.050 TYP	
L1	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

Package Outline Dimensions

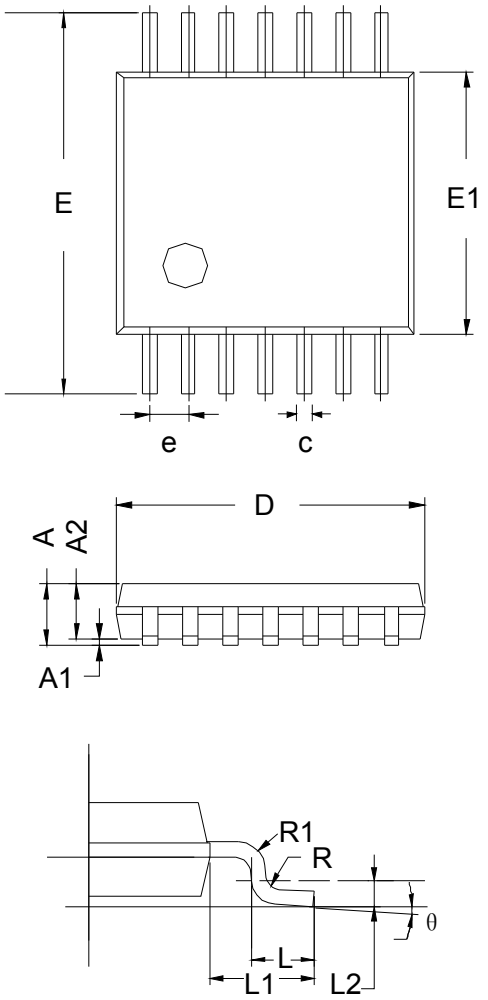
MSOP-8



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.800	1.200	0.031	0.047
A1	0.000	0.200	0.000	0.008
A2	0.760	0.970	0.030	0.038
b	0.30 TYP		0.012 TYP	
C	0.15 TYP		0.006 TYP	
D	2.900	3.100	0.114	0.122
e	0.65 TYP		0.026	
E	2.900	3.100	0.114	0.122
E1	4.700	5.100	0.185	0.201
L1	0.410	0.650	0.016	0.026
θ	0°	6°	0°	6°

Package Outline Dimensions

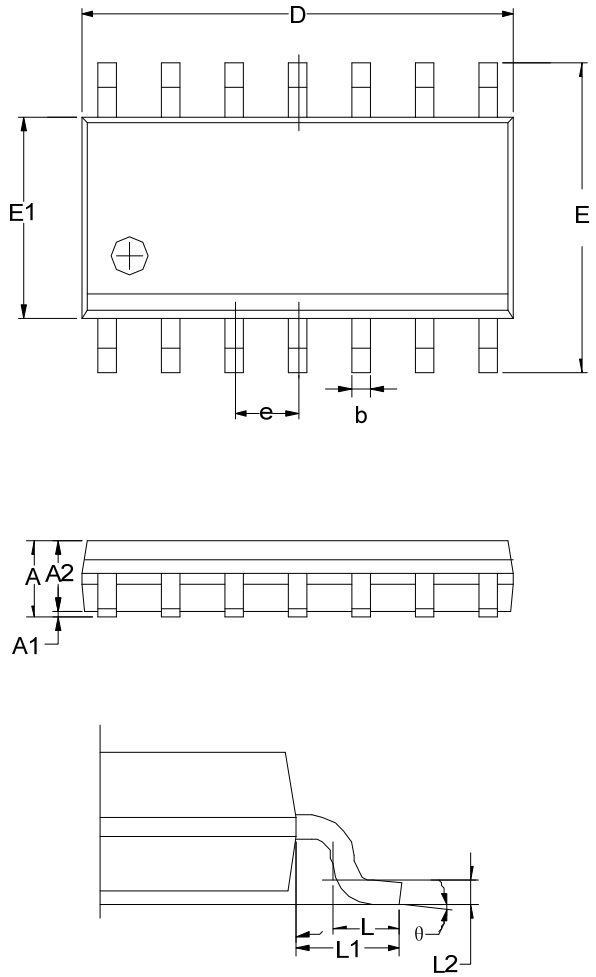
TSSOP-14



Symbol	Dimensions In Millimeters		
	MIN	TYP	MAX
A	-	-	1.20
A1	0.05	-	0.15
A2	0.90	1.00	1.05
b	0.20	-	0.28
c	0.10	-	0.19
D	4.86	4.96	5.06
E	6.20	6.40	6.60
E1	4.30	4.40	4.50
e	0.65 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		
L2	0.25 BSC		
R	0.09	-	-
θ	0°	-	8°

Package Outline Dimensions

SO-14 (SOIC-14)



Symbol	Dimensions In Millimeters		
	MIN	TYP	MAX
A	1.35	1.60	1.75
A1	0.10	0.15	0.25
A2	1.25	1.45	1.65
b	0.36		0.49
D	8.53	8.63	8.73
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.27 BSC		
L	0.45	0.60	0.80
L1	1.04 REF		
L2	0.25 BSC		
θ	0°		8°