

1. Description

The KIA30N06B is the highest performance trench N-ch MOSFETs with extreme high cell density, which provide excellent RDSON and gate charge for most of the synchronous buck converter applications. The KIA30N06B meet the RoHS and Green Product requirement, 100% EAS guaranteed with full function reliability approved.

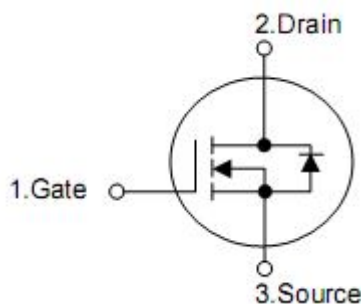
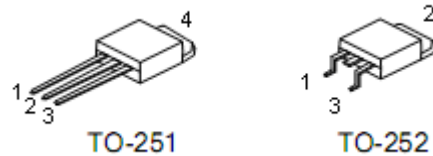
2. Features

- $R_{DS(on)}=25m\Omega @ V_{DS}=60V$
- Advanced high cell density Trench technology
- Super Low Gate Charge
- Excellent Cdv/dt effect decline
- 100% EAS Guaranteed
- Green Device Available

3. Applications

- High Frequency Point-of-Load Synchronous Buck Converter
- Networking DC-DC Power System
- Load Switch

4. Symbol



Pin	Function
1	Gate
2	Drain
3	Source
4	Drain

5. Absolute maximum ratings

Parameter	Symbol	Rating	Units
Drain-source voltage	V_{DS}	60	V
Gate-source voltage	V_{GS}	+20	V
Continuous drain current, $V_{GS}@10V^1$	I_D	$T_C=25^{\circ}C$	25
		$T_C=100^{\circ}C$	18
Pulsed drain current ²	I_{DM}	50	A
Single pulse avalanche energy ³	E_{AS}	34.5	mJ
Avalanche current	I_{AS}	22.6	A
Total power dissipation ⁴	P_D	34.7	W
$T_C=25^{\circ}C$			
Operation junction temperature range	T_J	-55 to 150	$^{\circ}C$
Storage temperature range	T_{STG}	-55 to 150	$^{\circ}C$

6. Thermal characteristics

Parameter	Symbol	Typ	Max	Unit
Thermal resistance, Junction-ambient ¹	$R_{\theta JA}$	--	62	$^{\circ}C/W$
Thermal resistance, Junction-case ¹	$R_{\theta JC}$	--	3.6	

7. Electrical characteristics

($T_J=25^{\circ}\text{C}$, unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Drain-source breakdown voltage	BV_{DSS}	$V_{GS}=0V, I_D=250\mu A$	60	-	-	V
BV_{DSS} temperature coefficient	$\Delta BV_{DSS}/\Delta T_J$	Reference to 25°C , $I_D=1\text{mA}$		0.063		$V/^{\circ}\text{C}$
Static drain-source on-resistance ²	$R_{DS(on)}$	$V_{GS}=10V, I_D=15A$		25	30	m Ω
		$V_{GS}=4.5V, I_D=10A$		30	38	
Gate threshold voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	1.2		2.5	V
$V_{GS(th)}$ temperature coefficient	$\Delta V_{GS(th)}$			-5.24		$\text{mV}/^{\circ}\text{C}$
Drain-source leakage current	I_{DSS}	$V_{DS}=48V, V_{GS}=0V$ $T_J=25^{\circ}\text{C}$			1	μA
		$V_{DS}=48V, V_{GS}=0V$ $T_J=55^{\circ}\text{C}$			5	μA
Gate- source leakage current	I_{GSS}	$V_{GS}=\pm 20V, V_{DS}=0V$			± 100	nA
Forward transconductance	g_{fs}	$V_{DS}=5V, I_D=15A$		17		S
Gate resistance	R_g	$V_{DS}=0V, V_{GS}=0V, f=1\text{MHz}$		3.2		Ω
Total gate charge(4.5V)	Q_g	$V_{DS}=48V, V_{GS}=4.5V$ $I_D=10A$	-	12.56		nC
Gate-source charge	Q_{gs}			3.24		
Gate-drain charge	Q_{gd}			6.31		
Turn-on delay time	$t_{d(on)}$	$V_{DD}=30V, I_D=10A,$ $R_G=3.3\Omega, V_{GS}=10V$		8		ns
Rise time	t_r			14.2		
Turn-off delay time	$t_{d(off)}$			24.4		
Fall time	t_f			4.6		
Input capacitance	C_{iss}	$V_{DS}=25V, V_{GS}=0V,$ $f=1\text{MHz}$		1345		pF
Output capacitance	C_{oss}			72.5		
Reverse transfer capacitance	C_{rss}			54.4		
Single pulse avalanche energy ⁵	EAS	$V_{DD}=25V, L=0.1\text{mH},$ $I_{AS}=15A$	15.2			mJ
Continuous source current ^{1,6}	I_S	$V_G=V_D=0V,$ Force current			25	A
Pulsed source current ^{2,6}	I_{SM}				50	A
Diode forward voltage ²	V_{SD}	$V_{GS}=0V, I_S=1A, T_J=25^{\circ}\text{C}$			1.2	V

Note:1.The data tested by surface mounted on a 1 inch² FR-4 board with 20Z copper.

2.The data tested by pulsed, pulse width $\leq 300\mu\text{s}$, duty cycle $\leq 2\%$

3.The EAS data shows Max.rating.The test condition is $V_{DD}=25V, V_{GS}=10V, L=0.1\text{mH}, I_{AS}=15A$

4.The power dissipation is limited by 150°C junction temperature

5.The Min, value is 100% EAS tested guarantee.

6.The data is theoretically the same as I_D and I_{DM} , in real applications, should be limited by total power dissipation.

8. Test circuits and waveforms

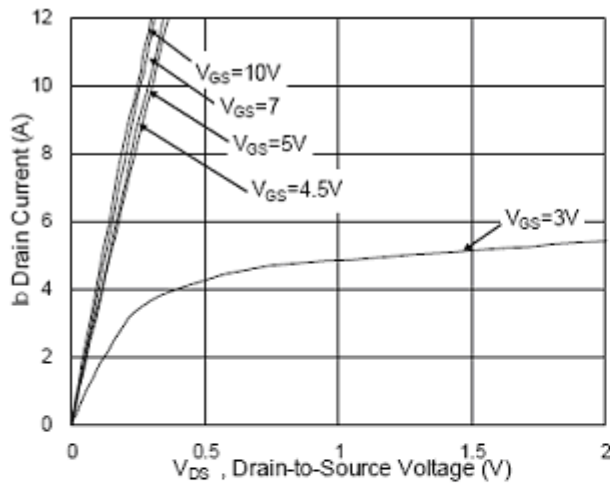


Fig.1 Typical Output Characteristics

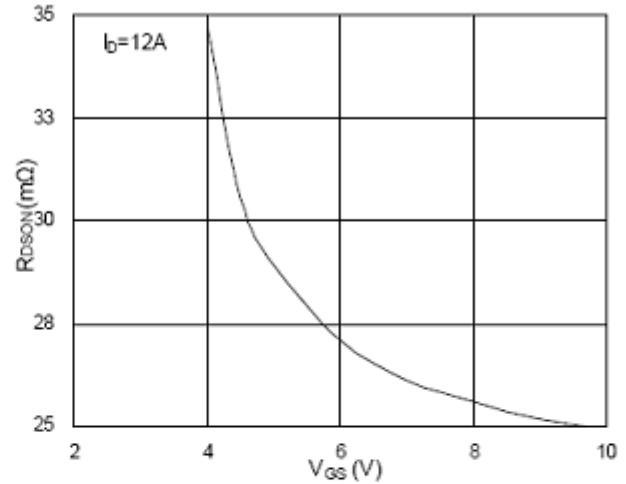


Fig.2 On-Resistance v.s. Gate-Source

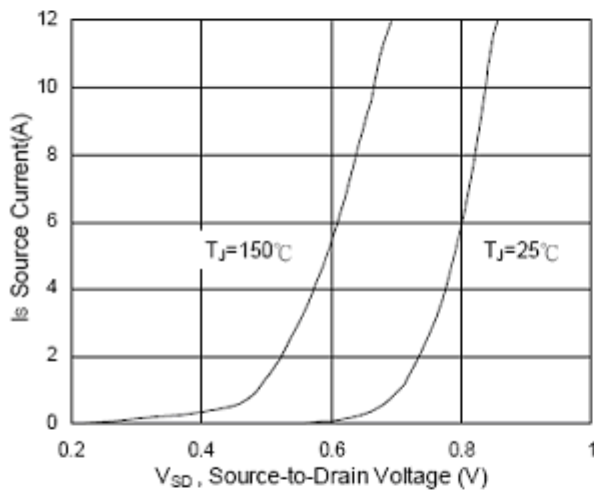


Fig.3 Forward Characteristics of Reverse

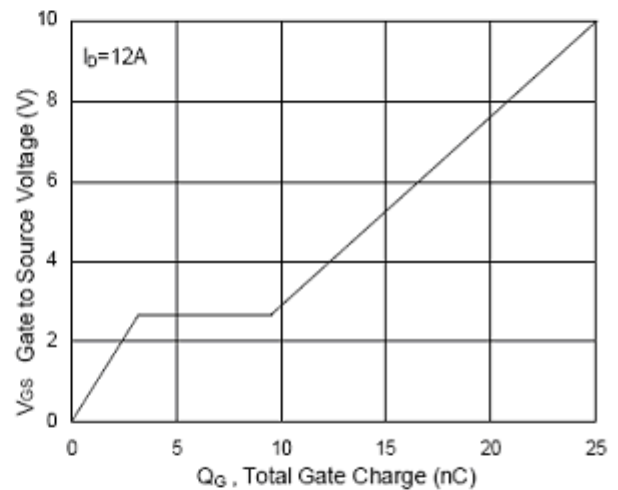


Fig.4 Gate-Charge characteristics

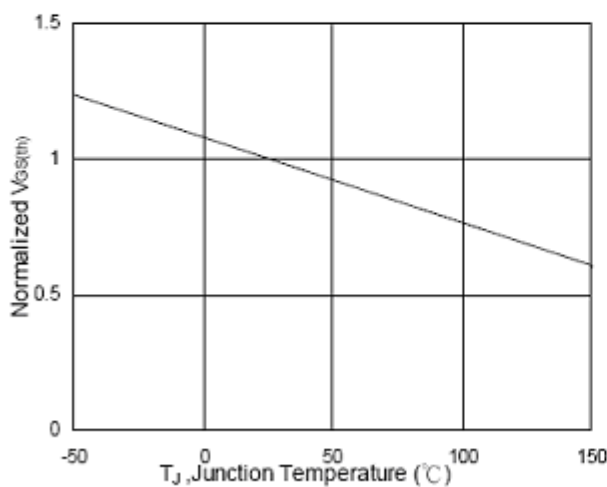


Fig.5 Normalized $V_{GS(th)}$ v.s T_J

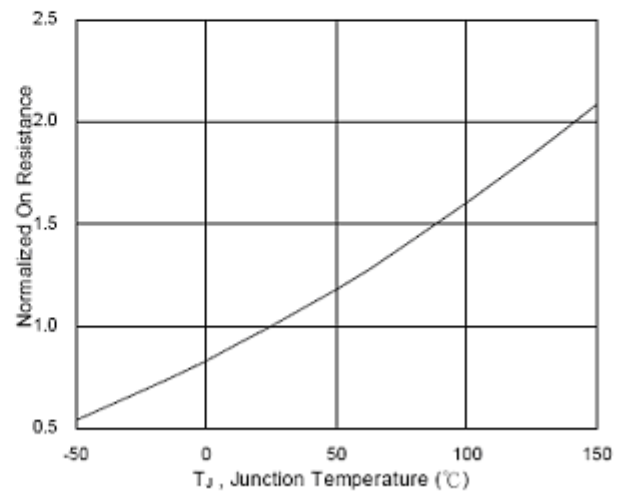


Fig.6 Normalized $R_{DS(on)}$ v.s T_J

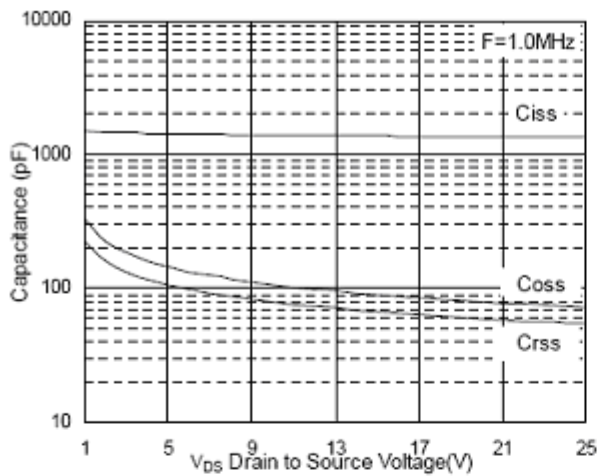


Fig.7 Capacitance

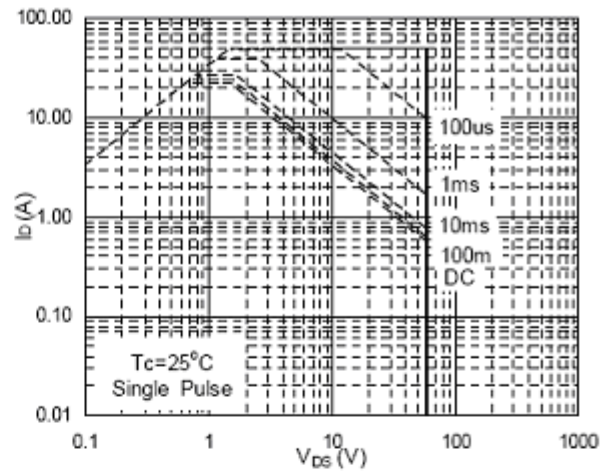


Fig.8 Safe Operating Area

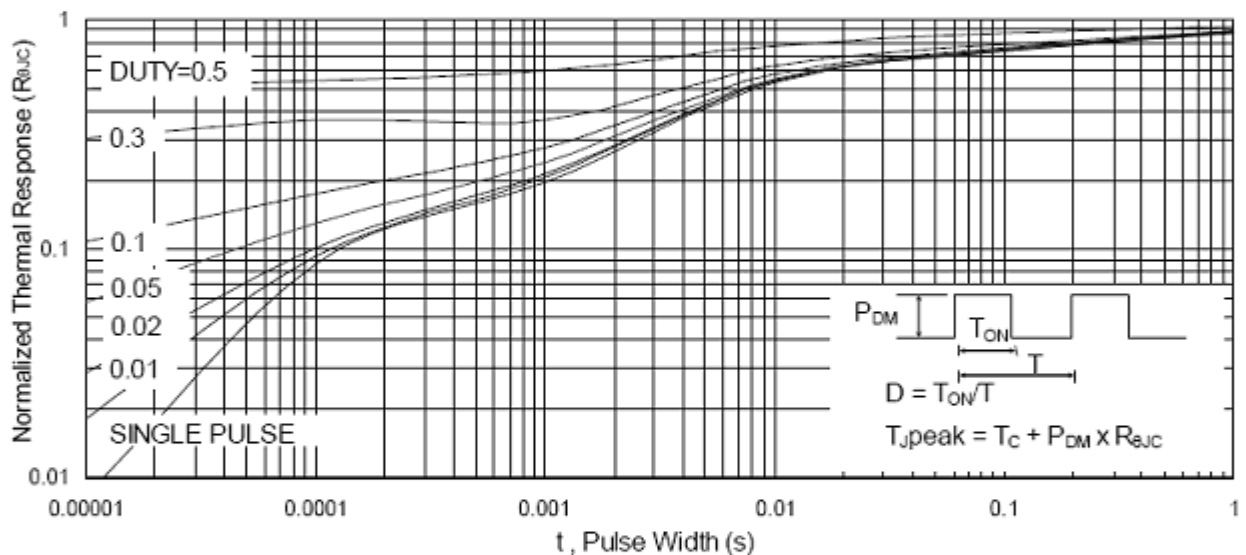


Fig.9 Normalized Maximum Transient Thermal Impedance

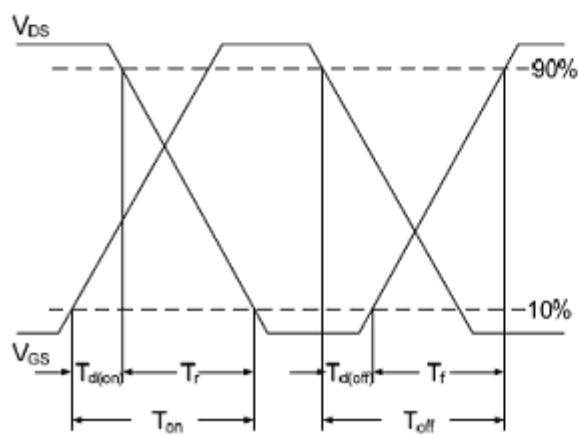


Fig.10 Switching Time Waveform

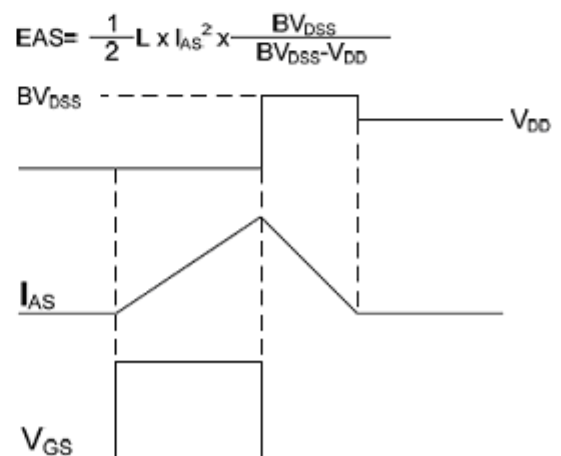


Fig.11 Unclamped Inductive Waveform