TXB0104 4-Bit Bidirectional Voltage-level Translator With Automatic Direction Sensing and ±15-kV ESD Protection

1 Features

- 1.2-V to 3.6-V on A Port and 1.65-V to 5.5-V on B Port ($V_{CCA} \leq V_{CCB}$)
- V_{CC} Isolation Feature: If Either V_{CC} Input Is at GND, All Outputs Are in the High-Impedance State
- Output Enable (OE) Input Circuit Referenced to V_{CCA}
- Low Power Consumption, 5-µA Maximum I_{CC}
- I_{OFF} Supports Partial Power-Down Mode Operation
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - A Port:
    - 2500-V Human-Body Model (A114-B)
    - 1500-V Charged-Device Model (C101)
  - B Port:
    - ±15-kV Human-Body Model (A114-B)
    - 1500-V Charged-Device Model (C101)

2 Applications

- Headsets
- Smartphones
- Tablets
- Desktop PC

3 Description

This TXB0104 4-bit noninverting translator uses two separate configurable power-supply rails. The A port is designed to track V_{CCA}. V_{CCA} accepts any supply voltage from 1.2 V to 3.6 V. The B port is designed to track V_{CCB}. V_{CCB} accepts any supply voltage from 1.65 V to 5.5 V. This allows for universal low-voltage bidirectional translation between any of the 1.2-V, 1.5-V, 1.8-V, 2.5-V, 3.3-V, and 5-V voltage nodes. V_{CCA} must not exceed V_{CCB}.

When the OE input is low, all outputs are placed in the high-impedance state. To ensure the high-impedance state during power up or power down, OE must be tied to GND through a pulldown resistor The current sourcing capability of the driver determines the minimum value of the resistor.

The TXB0104 device is designed so the OE input circuit is supplied by V_{CCA}.

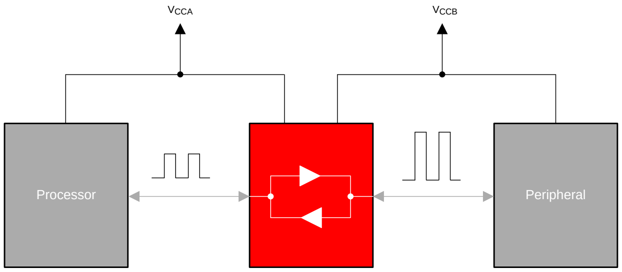
This device is fully specified for partial power-down applications using I_{OFF}. The I_{OFF} circuitry disables the outputs, which prevents damaging current backflow through the device when the device is powered down.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TXB0104RUT	UQFN (12)	2.00 mm × 1.70 mm
TXB0104D	SOIC (14)	8.65 mm × 3.91 mm
TXB0104ZXU/GXU	BGA MICROSTAR JUNIOR™ (12)	2.00 mm × 2.50 mm
TXB0104PW	TSSOP (14)	5.00 mm × 4.40 mm
TXB0104RGY	VQFN (14)	3.50 mm × 3.50 mm
TXB0104YZT	DSBGA (12)	1.40 mm × 1.90 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application Block Diagram for TXB010X



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

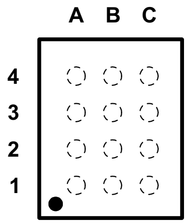
Changes from Revision H (Janurary 2018) to Revision I	Page
• Updated *Pin Functions* table	4
• Added *Pin Assignments* table for GXU and ZXU package	4
• Added *Pin Assignments* table for YZT package	4
• Updated *Layout Example*	22

Changes from Revision G (November 2014) to Revision H	Page
• Added package families to package pinout drawings in *Pin Configuration and Functions* section	3
• Added junction temperature range in *Absolute Maximum Ratings*table	5
• Changed unit from V to kV in *ESD Ratings* table	5

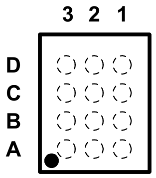
Changes from Revision F (May 2012) to Revision G	Page
• Added *Pin Configuration and Functions* section, *Handling Rating* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1

5 Pin Configuration and Functions

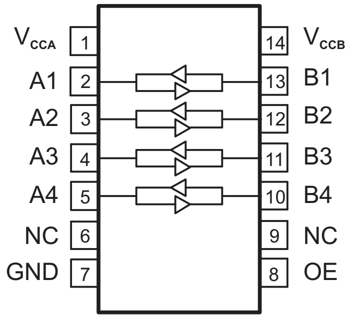
GXU and ZXU Package
12-Pin BGA Microstar Junior
Top View



YZT Package
12-Pin DSBGA
Top View

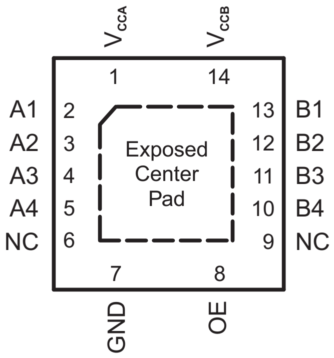


D or PW Package
14-Pin SOIC or TSSOP
Top View



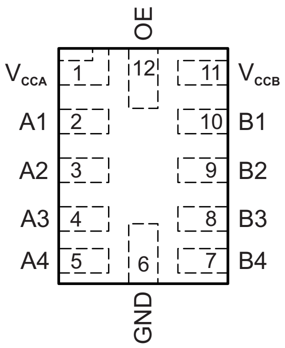
NC − No internal connection

RGY Package
14-Pin VQFN With Exposed Thermal Pad
Top View



NC − No internal connection

RUT Package
12-Pin UQFN
Top View



Pin Functions

PIN						I/O	DESCRIPTION
NAME	**D, PW**	**RGY**	**RUT**	**GXU, ZXU**	**YZT**		
A1	2	2	2	A1	A3	I/O	Input/output 1. Referenced to V_{CCA}.
A2	3	3	3	A2	B3	I/O	Input/output 2. Referenced to V_{CCA}.
A3	4	4	4	A3	C3	I/O	Input/output 3. Referenced to V_{CCA}.
A4	5	5	5	A4	D3	I/O	Input/output 4. Referenced to V_{CCA}.
B1	13	13	10	C1	A1	I/O	Input/output 1. Referenced to V_{CCB}.
B2	12	12	9	C2	B1	I/O	Input/output 2. Referenced to V_{CCB}.
B3	11	11	8	C3	C1	I/O	Input/output 3. Referenced to V_{CCB}.
B4	10	10	7	C4	D1	I/O	Input/output 4. Referenced to V_{CCB}.
GND	7	7	6	B4	D2	—	Ground
NC	6, 9	6,9	—	–	–	—	No connection. Not internally connected.
OE	8	8	12	B3	C2	I	Tri-state output-mode enable. Pull OE low to place all outputs in tri-state mode. Referenced to V_{CCA}.
V_{CCA}	1	1	1	B2	B2	—	A-port supply voltage 1.2 V ≤ V_{CCA} ≤ 3.6 V and V_{CCA} ≤ V_{CCB}.
V_{CCB}	14	14	11	B1	A2	—	B-port supply voltage 1.65 V ≤ V_{CCB} ≤ 5.5 V.
Thermal pad	—		—	–	–	—	For the RGY package, the exposed center thermal pad must either be connected to Ground or left electrically open.

Pin Assignments: GXU and ZXU Package

	A	**B**	**C**
4	A4	GND	B4
3	A3	OE	B3
2	A2	V_{CCA}	B2
1	A1	V_{CCB}	B1

Pin Assignments: YZT Package

	3	**2**	**1**
D	A4	GND	B4
C	A3	OE	B3
B	A2	V_{CCA}	B2
A	A1	V_{CCB}	B1

6 Specifications

6.1 Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Supply voltage, V_{CCA}		–0.5	4.6	V
Supply voltage, V_{CCB}		–0.5	6.5	
Input voltage, V_I	A port	–0.5	4.6	V
	B port	–0.5	6.5	
Voltage applied to any output in the high-impedance or power-off state, V_O	A port	–0.5	4.6	V
	B port	-0.5	6.5	
Voltage applied to any output in the high or low state, V_O (2)	A port	–0.5	V_{CCA} + 0.5	V
	B port	–0.5	V_{CCB} + 0.5	
Input clamp current, I_{IK}	$V_I < 0$		–50	mA
Output clamp current, I_{OK}	$V_O < 0$		–50	mA
Continuous output current, I_O		–50	50	mA
Continuous current through V_{CCA}, V_{CCB}, or GND		–100	100	mA
Junction temperature range, T_J			150	°C
Storage temperature range, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The value of V_{CCA} and V_{CCB} are provided in the recommended operating conditions table.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	A port	±2.5	kV
		Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	B port	±15	
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	A port	±1.5	
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	B port	±1.5	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)(2)

					MIN	**MAX**	**UNIT**
V_{CCA}	Supply voltage				1.2	3.6	V
V_{CCB}	Supply voltage				1.65	5.5	
V_{IH}	High-level input voltage	Data inputs	V_{CCA} = 1.2 V to 3.6 V V_{CCB} = 1.65 V to 5.5 V		V_{CCI} × 0.65(3)	V_{CCI}	V
		OE	V_{CCA} = 1.2 V to 3.6 V V_{CCB} = 1.65 V to 5.5 V		V_{CCA} × 0.65	5.5	
V_{IL}	Low-level input voltage	Data inputs	V_{CCA} = 1.2 V to 5.5 V V_{CCB} = 1.65 V to 5.5 V		0	V_{CCI} × 0.35(3)	V
		OE	V_{CCA} = 1.2 V to 3.6 V V_{CCB} = 1.65 V to 5.5 V		0	V_{CCA} × 0.35	
V_O	Voltage applied to any output in the high-impedance or power-off state	A-port	V_{CCA} = 1.2 V to 3.6 V V_{CCB} = 1.65 V to 5.5 V		0	3.6	V
		B-port	V_{CCA} = 1.2 V to 3.6 V V_{CCB} = 1.65 V to 5.5 V		0	5.5	
Δt/Δv	Input transition rise or fall rate	A-port inputs	V_{CCA} = 1.2 V to 3.6 V V_{CCB} = 1.65 V to 5.5 V			40	ns/V
		B-port inputs	V_{CCA} = 1.2 V to 3.6 V	V_{CCB} = 1.65 V to 3.6 V		40	
				V_{CCB} = 4.5 V to 5.5 V		30	
T_A	Operating free-air temperature				–40	85	°C

(1) The A and B sides of an unused data I/O pair must be held in the same state, that is, both at V_{CCI} or both at GND.
(2) V_{CCA} must be less than or equal to V_{CCB} and must not exceed 3.6 V.
(3) V_{CCI} is the supply voltage associated with the input port.

6.4 Thermal Information

THERMAL METRIC(1)		**TXB0104**						**UNIT**
		D	**GXU/ZXU**	**PW**	**RGY**	**RUT**	**YZT**	
		14 PINS	**12 PINS**	**14 PINS**	**14 PINS**	**12 PINS**	**12 PINS**	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	90.7	127.1	121.0	52.8	119.8	89.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	50.5	92.8	50.0	67.7	42.6	0.9	
$R_{\theta JB}$	Junction-to-board thermal resistance	45.4	62.2	62.8	28.9	52.5	14.4	
ψ_{JT}	Junction-to-top characterization parameter	14.7	2.3	6.4	2.6	0.7	3.0	
ψ_{JB}	Junction-to-board characterization parameter	45.1	62.2	62.2	29.0	52.3	14.4	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	–	–	–	–	–	–	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics(1)(2)

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CCA}	V_{CCB}	T_A = 25°C			–40°C to 85°C		UNIT
					MIN	TYP	MAX	MIN	MAX	
V_{OHA}	Port A output high voltage	I_{OH} = –20 µA	1.2 V			1.1				V
			1.4 V to 3.6 V					V_{CCA} – 0.4		
V_{OLA}	Port A output low voltage	I_{OL} = 20 µA	1.2 V			0.3				V
			1.4 V to 3.6 V						0.4	
V_{OHB}	Port B output high voltage	I_{OH} = –20 µA		1.65 V to 5.5 V				V_{CCB} – 0.4		V
V_{OLB}	Port B output low voltage	I_{OL} = 20 µA		1.65 V to 5.5 V					0.4	V
I_I	Inflection-point current	OE: V_I = V_{CCI} or GND	1.2 V to 3.6 V	1.65 V to 5.5 V	–1		1	–2	2	µA
I_{off}	Off-state current	A port: V_I or V_O = 0 to 3.6 V	0 V	0 V to 5.5 V	–1		1	–2	2	µA
		B port: V_I or V_O = 0 to 5.5 V	0 V to 3.6 V	0 V	–1		1	–2	2	
I_{OZ}	High-impedance-state output current	A or B port: OE = GND	1.2 V to 3.6 V	1.65 V to 5.5 V	–1		1	–2	2	µA
I_{CCA}	V_{CCA} supply current	V_I = V_{CCI} or GND I_O = 0	1.2 V	1.65 V to 5.5 V		0.06				µA
			1.4 V to 3.6 V	1.65 V to 5.5 V					5	
			3.6 V	0 V					2	
			0 V	5.5 V					–2	
I_{CCB}	V_{CCB} supply current	V_I = V_{CCI} or GND I_O = 0	1.2 V	1.65 V to 5.5 V		3.4				µA
			1.4 V to 3.6 V	1.65 V to 5.5 V					5	
			3.6 V	0 V					–2	
			0 V	5.5 V					2	
I_{CCA} + I_{CCB}	Combined supply current	V_I = V_{CCI} or GND I_O = 0	1.2 V	1.65 V to 5.5 V		3.5				µA
			1.4 V to 3.6 V	1.65 V to 5.5 V					10	
I_{CCZA}	High-impedance state, V_{CCA} supply current	V_I = V_{CCI} or GND I_O = 0, OE = GND	1.2 V	1.65 V to 5.5 V		0.05				µA
			1.4 V to 3.6 V	1.65 V to 5.5 V					5	
I_{CCZB}	High-impedance state, V_{CCB} supply current	V_I = V_{CCI} or GND I_O = 0, OE = GND	1.2 V	1.65 V to 5.5 V		3.3				µA
			1.4 V to 3.6 V	1.65 V to 5.5 V					5	
C_i	Input capacitance	OE	1.2 V to 3.6 V	1.65 V to 5.5 V		3			4	pF
C_{io}	Input-to-output internal capacitance	A port	1.2 V to 3.6 V	1.65 V to 5.5 V		5			6	pF
		B port	1.2 V to 3.6 V	1.65 V to 5.5 V		11			14	

(1) V_{CCI} is the supply voltage associated with the input port.
(2) V_{CCO} is the supply voltage associated with the output port.

6.6 Timing Requirements: V_{CCA} = 1.2 V

T_A = 25°C, V_{CCA} = 1.2 V

			V_{CCB} = 1.8 V			V_{CCB} = 2.5 V			V_{CCB} = 3.3 V			V_{CCB} = 5 V			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
	Data rate			20			20			20			20		Mbps
t_w	Pulse duration	Data inputs		50			50			50			50		ns

6.7 Timing Requirements: V_{CCA} = 1.5 V ± 0.1 V

over recommended operating free-air temperature range, V_{CCA} = 1.5 V ± 0.1 V (unless otherwise noted)

			V_{CCB} = 1.8 V ± 0.15 V		V_{CCB} = 2.5 V ± 0.2 V		V_{CCB} = 3.3 V ± 0.3 V		V_{CCB} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
	Data rate			40		40		40		40	Mbps
t_w	Pulse duration	Data inputs	25		25		25		25		ns

6.8 Timing Requirements: V_{CCA} = 1.8 V ± 0.15 V

over recommended operating free-air temperature range, V_{CCA} = 1.8 V ± 0.15 V (unless otherwise noted)

			V_{CCB} = 1.8 V ± 0.15 V		V_{CCB} = 2.5 V ± 0.2 V		V_{CCB} = 3.3 V ± 0.3 V		V_{CCB} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
	Data rate			60		60		60		60	Mbps
t_w	Pulse duration	Data inputs	17		17		17		17		ns

6.9 Timing Requirements: V_{CCA} = 2.5 V ± 0.2 V

over recommended operating free-air temperature range, V_{CCA} = 2.5 V ± 0.2 V (unless otherwise noted)

			V_{CCB} = 2.5 V ± 0.2 V		V_{CCB} = 3.3 V ± 0.3 V		V_{CCB} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
	Data rate			100		100		100	Mbps
t_w	Pulse duration	Data inputs	10		10		10		ns

6.10 Timing Requirements: V_{CCA} = 3.3 V ± 0.3 V

over recommended operating free-air temperature range, V_{CCA} = 3.3 V ± 0.3 V (unless otherwise noted)

			V_{CCB} = 3.3 V ± 0.3 V		V_{CCB} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	
	Data rate			100		100	Mbps
t_w	Pulse duration	Data inputs	10		10		ns

6.11 Switching Characteristics: V_{CCA} = 1.2 V

T_A = 25°C, V_{CCA} = 1.2 V

PARAMETER		TEST CONDITIONS	V_{CCB} = 1.8 V			V_{CCB} = 2.5 V			V_{CCB} = 3.3 V			V_{CCB} = 5 V			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t_{pd}	Propagation delay time	A-to-B		6.9			5.7			5.3			5.5		ns
		B-to-A		7.4			6.4			6			5.8		
t_{en}	Enable time	OE-to-A		1			1			1			1		µs
		OE-to-B		1			1			1			1		
t_{dis}	Disable time	OE-to-A		18			15			14			14		ns
		OE-to-B		20			17			16			16		
t_{rA}, t_{fA}	Input rise time, input fall time	A-port rise and fall times		4.2			4.2			4.2			4.2		ns
t_{rB}, t_{fB}	Input rise time, input fall time	B-port rise and fall times		2.1			1.5			1.2			1.1		ns
$t_{SK(O)}$	Skew (time), output	Channel-to-channel skew		0.4			0.5			0.5			1.4		ns
	Maximum data rate			20			20			20			20		Mbps

6.12 Switching Characteristics: V_{CCA} = 1.5 V ± 0.1 V

over recommended operating free-air temperature range, V_{CCA} = 1.5 V ± 0.1 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CCB} = 1.8 V ± 0.15 V		V_{CCB} = 2.5 V ± 0.2 V		V_{CCB} = 3.3 V ± 0.3 V		V_{CCB} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	Propagation delay time	A-to-B	1.4	12.9	1.2	10.1	1.1	10	0.8	9.9	ns
		B-to-A	0.9	14.2	0.7	12	0.4	11.7	0.3	13.7	
t_{en}	Enable time	OE-to-A		1		1		1		1	µs
		OE-to-B		1		1		1		1	
t_{dis}	Disable time	OE-to-A	5.9	31	5.7	25.9	5.6	23	5.7	22.4	ns
		OE-to-B	5.4	30.3	4.9	22.8	4.8	20	4.9	19.5	
t_{rA}, t_{fA}	Input rise time, input fall time	A-port rise and fall times	1.4	5.1	1.4	5.1	1.4	5.1	1.4	5.1	ns
t_{rB}, t_{fB}	Input rise time, input fall time	B-port rise and fall times	0.9	4.5	0.6	3.2	0.5	2.8	0.4	2.7	ns
$t_{SK(O)}$	Skew (time), output	Channel-to-channel skew		0.5		0.5		0.5		0.5	ns
	Maximum data rate		40		40		40		40		Mbps

6.13 Switching Characteristics: V_{CCA} = 1.8 V ± 0.15 V

over recommended operating free-air temperature range, V_{CCA} = 1.8 V ± 0.15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CCB} = 1.8 V ± 0.15 V		V_{CCB} = 2.5 V ± 0.2 V		V_{CCB} = 3.3 V ± 0.3 V		V_{CCB} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	Propagation delay time	A-to-B	1.6	11	1.4	7.7	1.3	6.8	1.2	6.5	ns
		B-to-A	1.5	12	1.3	8.4	1	7.6	0.9	7.1	
t_{en}	Enable time	OE-to-A		1		1		1		1	µs
		OE-to-B		1		1		1		1	
t_{dis}	Disable time	OE-to-A	5.9	31	5.1	21.3	5	19.3	5	17.4	ns
		OE-to-B	5.4	30.3	4.4	20.8	4.2	17.9	4.3	16.3	
t_{rA}, t_{fA}	Input rise time, input fall time	A-port rise and fall times	1	4.2	1.1	4.1	1.1	4.1	1.1	4.1	ns
t_{rB}, t_{fB}	Input rise time, input fall time	B-port rise and fall times	0.9	3.8	0.6	3.2	0.5	2.8	0.4	2.7	ns
$t_{SK(O)}$	Skew (time), output	Channel-to-channel skew		0.5		0.5		0.5		0.5	ns
	Maximum data rate		60		60		60		60		Mbps

6.14 Switching Characteristics: V_{CCA} = 2.5 V ± 0.2 V

over recommended operating free-air temperature range, V_{CCA} = 2.5 V ± 0.2 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CCB} = 2.5 V ± 0.2 V		V_{CCB} = 3.3 V ± 0.3 V		V_{CCB} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	Propagation delay time	A-to-B	1.1	6.3	1	5.2	0.9	4.7	ns
		B-to-A	1.2	6.6	1.1	5.1	0.9	4.4	
t_{en}	Enable time	OE-to-A		1		1		1	µs
		OE-to-B		1		1		1	
t_{dis}	Disable time	OE-to-A	5.1	21.3	4.6	15.2	4.6	13.2	ns
		OE-to-B	4.4	20.8	3.8	16	3.9	13.9	
t_{rA}, t_{fA}	Input rise time, input fall time	A-port rise and fall times	0.8	3	0.8	3	0.8	3	ns
t_{rB}, t_{fB}	Input rise time, input fall time	B-port rise and fall times	0.7	2.6	0.5	2.8	0.4	2.7	ns
$t_{SK(O)}$	Skew (time), output	Channel-to-channel skew		0.5		0.5		0.5	ns
	Maximum data rate		100		100		100		Mbps

6.15 Switching Characteristics: V_{CCA} = 3.3 V ± 0.3 V

over recommended operating free-air temperature range, V_{CCA} = 3.3 V ± 0.3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CCB} = 3.3 V ± 0.3 V		V_{CCB} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	
t_{pd}	Propagation delay time	A-to-B	0.9	4.7	0.8	4	ns
		B-to-A	1	4.9	0.9	3.8	
t_{en}	Enable time	OE-to-A		1		1	μs
		OE-to-B		1		1	
t_{dis}	Disable time	OE-to-A	4.6	15.2	4.3	12.1	ns
		OE-to-B	3.8	16	3.4	13.2	
t_{rA}, t_{fA}	Input rise time, input fall time	A-port rise and fall times	0.7	2.5	0.7	2.5	ns
t_{rB}, t_{fB}	Input rise time, input fall time	B-port rise and fall times	0.5	2.1	0.4	2.7	ns
$t_{SK(O)}$	Skew (time), output	Channel-to-channel skew		0.5		0.5	ns
	Maximum data rate		100		100		Mbps

6.16 Operating Characteristics: V_{CCA} = 1.2 V to 1.5 V, V_{CCB} = 1.5 V to 1.8 V

T_A = 25°C

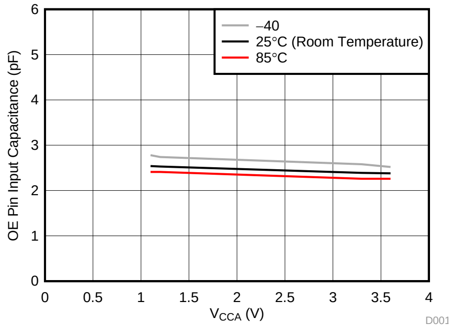
PARAMETER		TEST CONDITIONS		V_{CCA} = 1.2 V, V_{CCB} =1.5 V			V_{CCA} = 1.2 V, V_{CCB} = 1.8 V			V_{CCA} = 1.5 V, V_{CCB} = 1.8 V			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
C_{pdA}	Power dissipation capacitance	C_L = 0 f = 10 MHz t_r = t_f = 1 ns OE = V_{CCA} (outputs enabled)	A-port input, B-port output		7.8			10			9		pF
			B-port input, A-port output		12			11			11		
C_{pdB}	Power dissipation capacitance		A-port input, B-port output		38.1			28			28		
			B-port input, A-port output		25.4			19			18		
C_{pdA}	Power dissipation capacitance	C_L = 0 f = 10 MHz t_r = t_f = 1 ns OE = GND (outputs disabled)	A-port input, B-port output		0.01			0.01			0.01		pF
			B-port input, A-port output		0.01			0.01			0.01		
C_{pdB}	Power dissipation capacitance		A-port input, B-port output		0.01			0.01			0.01		
			B-port input, A-port output		0.01			0.01			0.01		

6.17 Operating Characteristics: V_{CCA} = 1.8 V to 3.3 V, V_{CCB} = 1.8 V to 5 V

T_A = 25°C

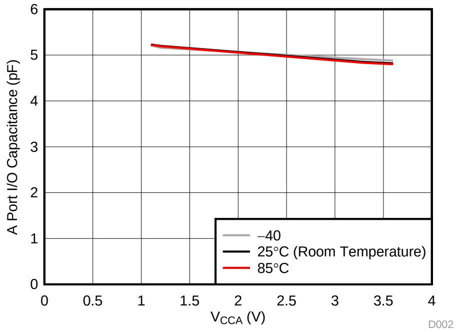
PARAMETER		TEST CONDITIONS		V_{CCA} = 1.8 V, V_{CCB} =1.8 V			V_{CCA} = 2.5 V, V_{CCB} = 2.5 V			V_{CCA} = 2.5 V, V_{CCB} = 5 V			V_{CCA} = 3.3 V, V_{CCB} = 3.3 V to 5 V			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
C_{pdA}	Power dissipation capacitance	C_L = 0 f = 10 MHz t_r = t_f = 1 ns OE = V_{CCA} (outputs enabled)	A-port input, B-port output		8			8			8			9		pF
			B-port input, A-port output		11			11			11			11		
C_{pdB}	Power dissipation capacitance		A-port input, B-port output		28			29			29			29		
			B-port input, A-port output		18			19			21			22		
C_{pdA}	Power dissipation capacitance	C_L = 0 f = 10 MHz t_r = t_f = 1 ns OE = GND (outputs disabled)	A-port input, B-port output		0.01			0.01			0.01			0.01		pF
			B-port input, A-port output		0.01			0.01			0.01			0.01		
C_{pdB}	Power dissipation capacitance		A-port input, B-port output		0.01			0.01			0.01			0.03		
			B-port input, A-port output		0.01			0.01			0.01			0.04		

6.18 Typical Characteristics



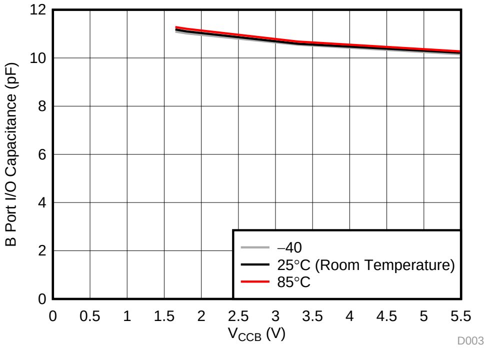
V_{CCB}= 3.3 V

Figure 1. Input Capacitance for OE Pin (C_I) vs Power Supply (V_{CCA})



V_{CCB}= 3.3 V

Figure 2. Capacitance for A port I/O Pins (C_{iO}) vs Power Supply (V_{CCA})



V_{CCA}= 1.8 V

Figure 3. Capacitance for B Port I/O Pins (C_{iO}) vs Power Supply (V_{CCB})

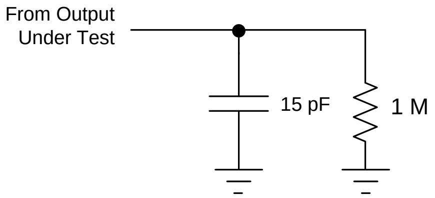
7 Parameter Measurement Information

Unless otherwise noted, all input pulses are supplied by generators that have the following characteristics:

- PRR 10 MHz
- Z_O = 50 W
- dv/dt ≥ 1 V/ns

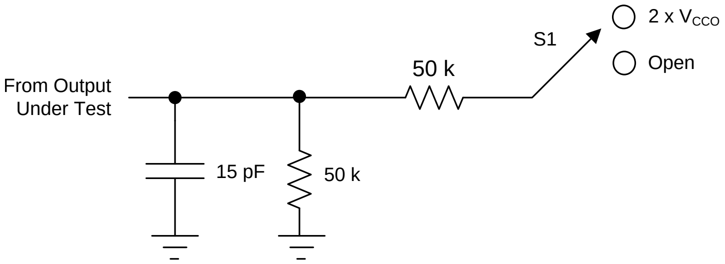
NOTE

All parameters and waveforms are not applicable to all devices.



(1) The outputs are measured one at a time, with one transition per measurement.

Figure 4. Load Circuit For Maximum Data Rate: Pulse Duration, Propagation Delay Output Rise, And Fall Time Measurement

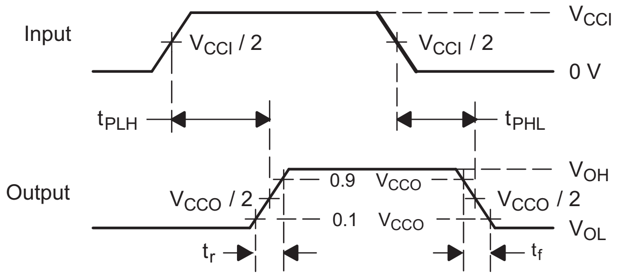


(1) The outputs are measured one at a time, with one transition per measurement.

Figure 5. Load Circuit For Enable / Disable Time Measurement

Table 1. Switch Position For Enable / Disable Time Measurement (See Figure 5)

TEST	S1
t_{PZL}, t_{PLZ}	2 × V_{CCO}
t_{PHZ}, t_{PZH}	Open



1. (1) V_{CCI} is the V_{CC} associated with the input port.
2. (2) V_{CCO} is the $_{VCC}$ associated with the output port.
3. (3) t_{PLH} and t_{PHL} are the same as t_{pd}.
4. (4) The outputs are measured one at a time, with one transition per measurement.

Figure 6. Voltage Waveforms Propagation Delay Times

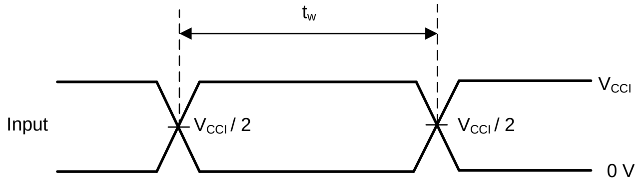


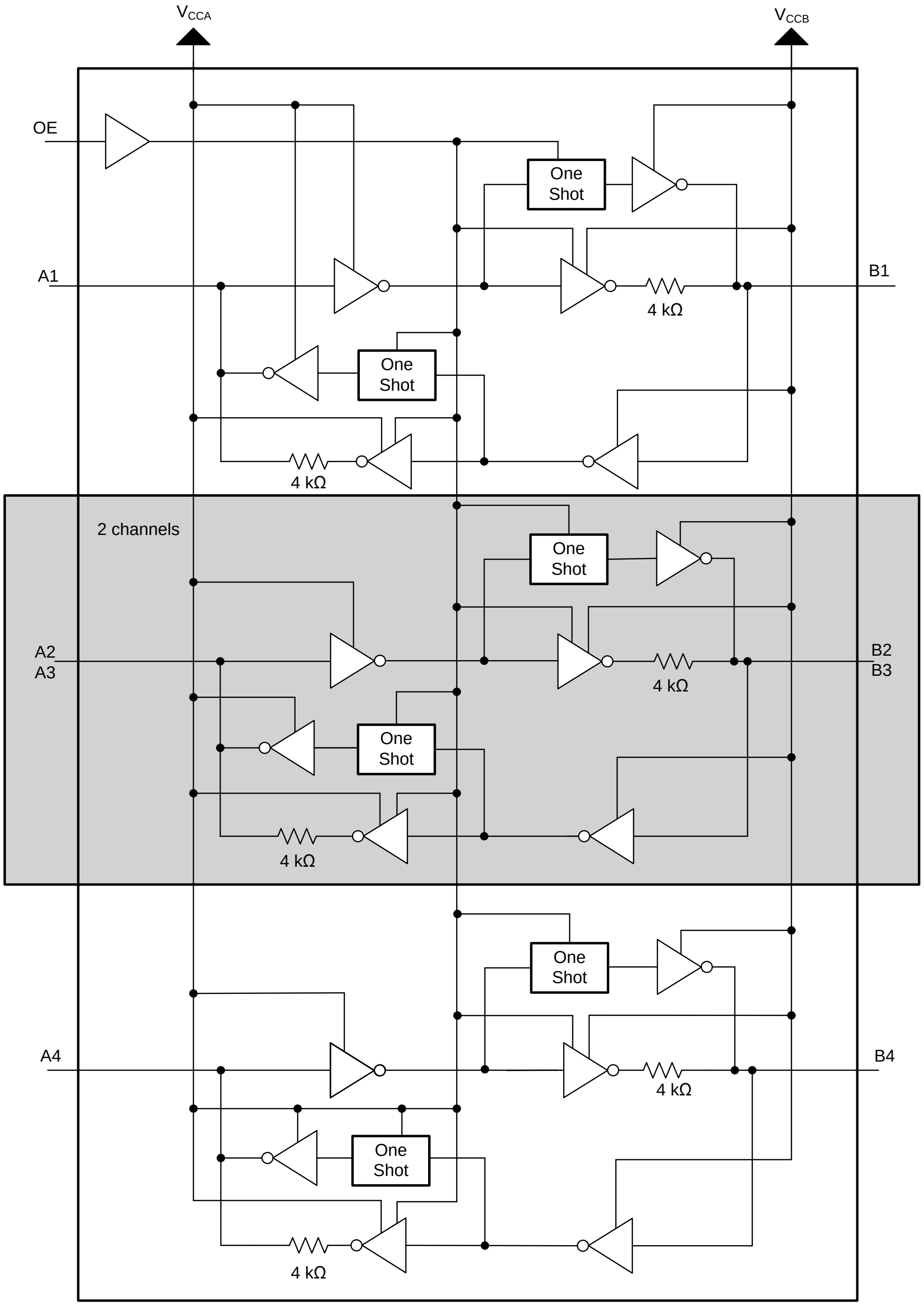
Figure 7. Voltage Waveforms Pulse Duration

8 Detailed Description

8.1 Overview

The TXB0104 device is a 4-bit, directionless voltage-level translator specifically designed for translating logic voltage levels. The A port is able to accept I/O voltages ranging from 1.2 V to 3.6 V, while the B port can accept I/O voltages from 1.65 V to 5.5 V. The device is a buffered architecture with edge-rate accelerators (one-shots) to improve the overall data rate. This device can only translate push-pull CMOS logic outputs. If for open-drain signal translation, please refer to TI's TXS010X products.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Architecture

The TXB0104 device architecture (see Figure 8) does not require a direction-control signal to control the direction of data flow from A to B or from B to A. In a DC state, the output drivers of the device maintain a high or low, but are designed to be weak, so the output drivers can be overdriven by an external driver when data on the bus flows the opposite direction.

The output one-shots detect rising or falling edges on the A or B ports. During a rising edge, the one-shot turns on the PMOS transistors (T1, T3) for a short duration, which speeds up the low-to-high transition. Similarly, during a falling edge, the one-shot turns on the NMOS transistors (T2, T4) for a short duration, which speeds up the high-to-low transition. The typical output impedance during output transition is 70 Ω at V_{CCO} = 1.2 V to 1.8 V, 50 Ω at V_{CCO} = 1.8 V to 3.3 V, and 40 Ω at V_{CCO} = 3.3 V to 5 V.

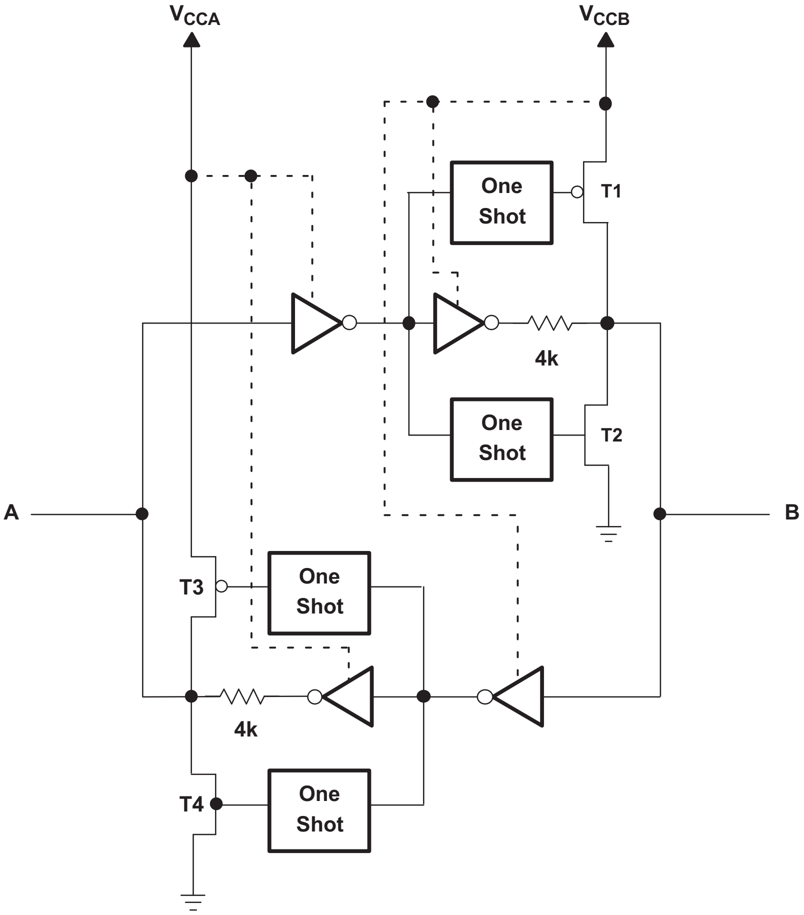
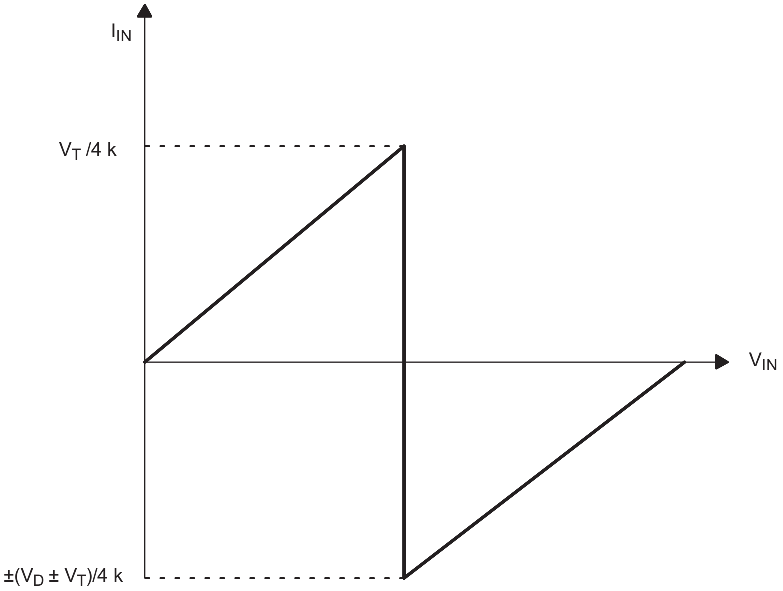


Figure 8. Architecture of TXB0104 Device I/O Cell

Feature Description (continued)

8.3.2 Input Driver Requirements

Typical I_{IN} vs V_{IN} characteristics of the device are shown in Figure 9. For proper operation, the device driving the data I/Os of the TXB0104 device must have drive strength of at least ±2 mA.



(1) V_T is the input threshold of the TXB0104 device, (typically V_{CC} / 2).

(2) V_D is the supply voltage of the external driver.

Figure 9. Typical I_{IN} vs V_{IN} Curve

8.3.3 Output Load Considerations

TI recommends careful PCB layout practices with short PCB trace lengths to avoid excessive capacitive loading and to ensure that proper O.S. triggering takes place. PCB signal trace-lengths must be kept short enough such that the round trip delay of any reflection is less than the one-shot duration. This improves signal integrity by ensuring that any reflection sees a low impedance at the driver. The O.S. circuits have been designed to stay on for approximately 10 ns. The maximum capacitance of the lumped load that can be driven also depends directly on the one-shot duration. With very heavy capacitive loads, the one-shot can time-out before the signal is driven fully to the positive rail. The O.S. duration has been set to best optimize trade-offs between dynamic ICC, load driving capability, and maximum bit-rate considerations. Both PCB trace length and connectors add to the capacitance that the device output sees, so it is recommended that this lumped-load capacitance be considered to avoid O.S. retriggering, bus contention, output signal oscillations, or other adverse system-level affects.

Feature Description (continued)

8.3.4 Enable and Disable

The TXB0104 device has an OE input that is used to disable the device by setting OE = low, which places all I/Os in the high-impedance (Hi-Z) state. The disable time (t_{dis}) indicates the delay between when OE goes low and when the outputs acutally get disabled (Hi-Z). The enable time (t_{en}) indicates the amount of time the user must allow for the one-shot circuitry to become operational after OE is taken high.

8.3.5 Pullup or Pulldown Resistors on I/O Lines

The device is designed to drive capacitive loads of up to 70 pF. The output drivers of the TXB0104 device have low dc drive strength. If pullup or pulldown resistors are connected externally to the data I/Os, their values must be kept higher than 50 kΩ to ensure that they do not contend with the output drivers of the TXB0104 device.

For the same reason, the TXB0104 device must not be used in applications such as I^2C or 1-Wire where an open-drain driver is connected on the bidirectional data I/O. For these applications, use a device from the TI TXS01xx series of level translators.

8.4 Device Functional Modes

The device has two functional modes, enabled and disabled. To disable the device, set the OE input to low, which places all I/Os in a high impedance state. Setting the OE input to high will enable the device.

9 Application and Implementation

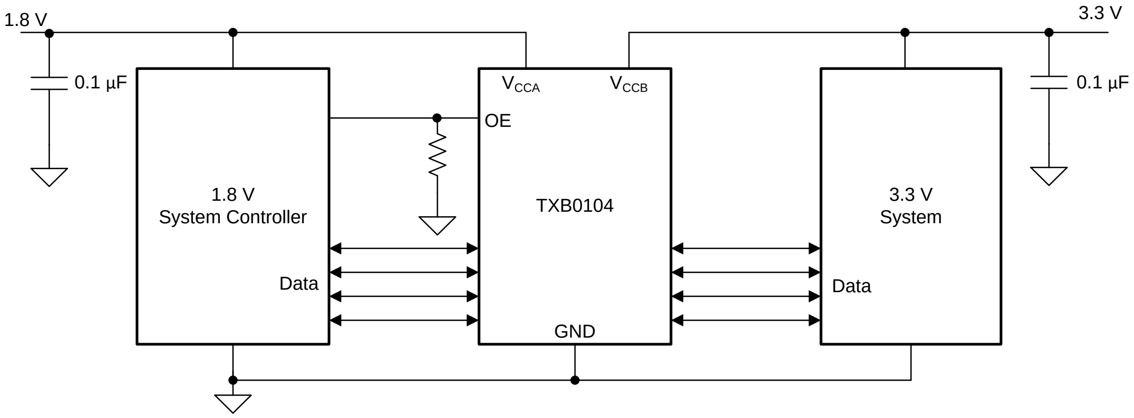
NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers must validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TXB0104 device can be used in level-translation applications for interfacing devices or systems operating at different interface voltages with one another. It can only translate push-pull CMOS logic outputs. If for open-drain signal translation, please refer to TI TXS010X products. Any external pulldown or pullup resistors are recommended larger than 50 kΩ.

9.2 Typical Application



9.2.1 Design Requirements

For this design example, use the parameters listed in Table 2. And make sure the $V_{CCA} \le V_{CCB}$.

Table 2. Design Parameters

DESIGN PARAMETERS	EXAMPLE VALUE
Input voltage range	1.2 V to 3.6 V
Output voltage range	1.65 V to 5.5 V

9.2.2 Detailed Design Procedure

To begin the design process, determine the following:

- Input voltage range
  - Use the supply voltage of the device that is driving the TXB0104 device to determine the input voltage range. For a valid logic high, the value must exceed the V_{IH} of the input port. For a valid logic low, the value must be less than the V_{IL} of the input port.
- Output voltage range
  - Use the supply voltage of the device that the device is driving to determine the output voltage range.
  - External pullup or pulldown resistors are not recommended. If mandatory, it is recommended that the value must be larger than 50 kΩ.
- An external pulldown or pullup resistor decreases the output V_{OH} and V_{OL}. Use the below equations to draft estimate the V_{OH} and V_{OL} as a result of an external pulldown and pullup resistor.

$$V_{OH} = V_{CCx} \times R_{PD} / (R_{PD} + 4.5\ k\Omega)$$

$$V_{OL} = V_{CCx} \times 4.5\ k\Omega / (R_{PU} + 4.5\ k\Omega)$$

Where

- V_{CCx} is the output port supply voltage on either V_{CCA} or V_{CCB}
- R_{PD} is the value of the external pull down resistor
- R_{PU} is the value of the external pull up resistor
- 4.5 kΩ is the counting the variation of the serial resistor 4 kΩ in the I/O line.

9.2.3 Application Curves

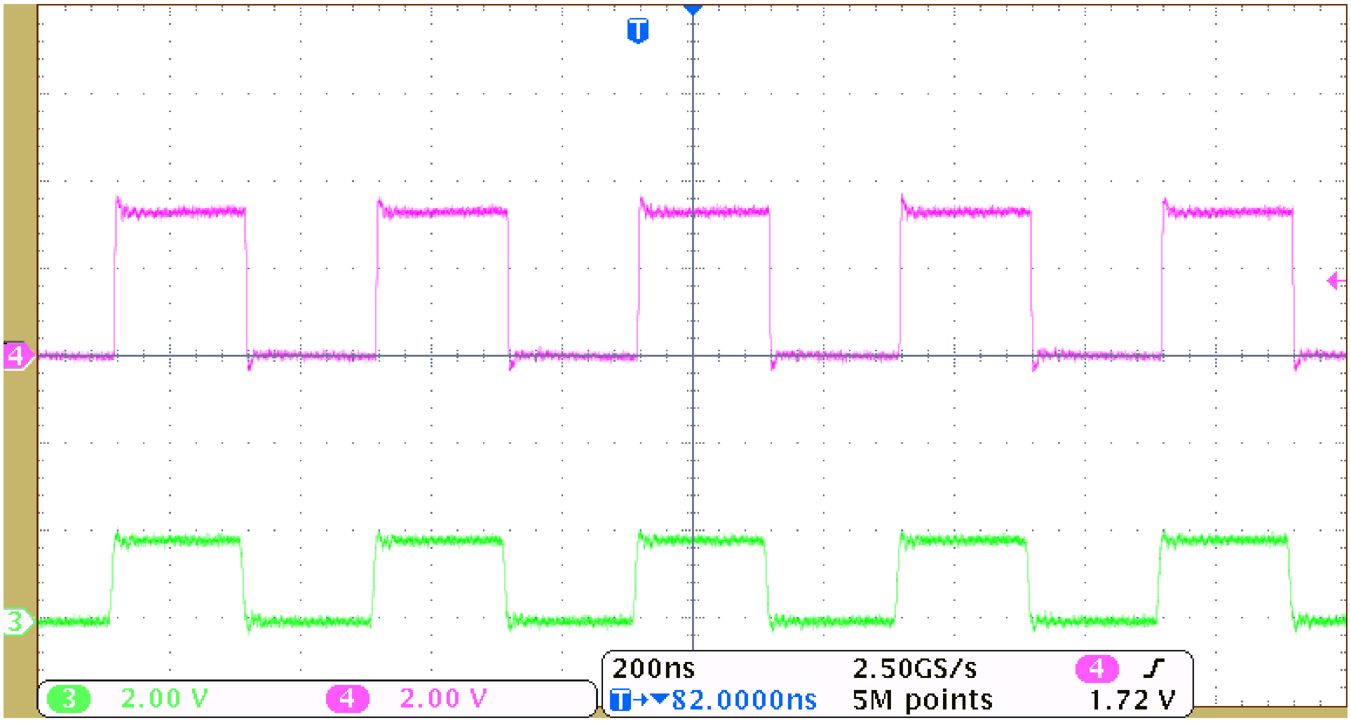


Figure 10. Level-Translation of a 2.5-MHz Signal

10 Power Supply Recommendations

During operation, ensure that V_{CCA} ≤ V_{CCB} at all times. During power-up sequencing, V_{CCA} ≥ V_{CCB} does not damage the device, so any power supply can be ramped up first. The device has circuitry that disables all output ports when either V_{CC} is switched off ($V_{CCA/B}$ = 0 V). The output-enable (OE) input circuit is designed so that it is supplied by V_{CCA} and when the (OE) input is low, all outputs are placed in the high-impedance state. To ensure the high-impedance state of the outputs during power up or power down, the OE input pin must be tied to GND through a pulldown resistor and must not be enabled until V_{CCA} and V_{CCB} are fully ramped and stable. The minimum value of the pulldown resistor to ground is determined by the current-sourcing capability of the driver.

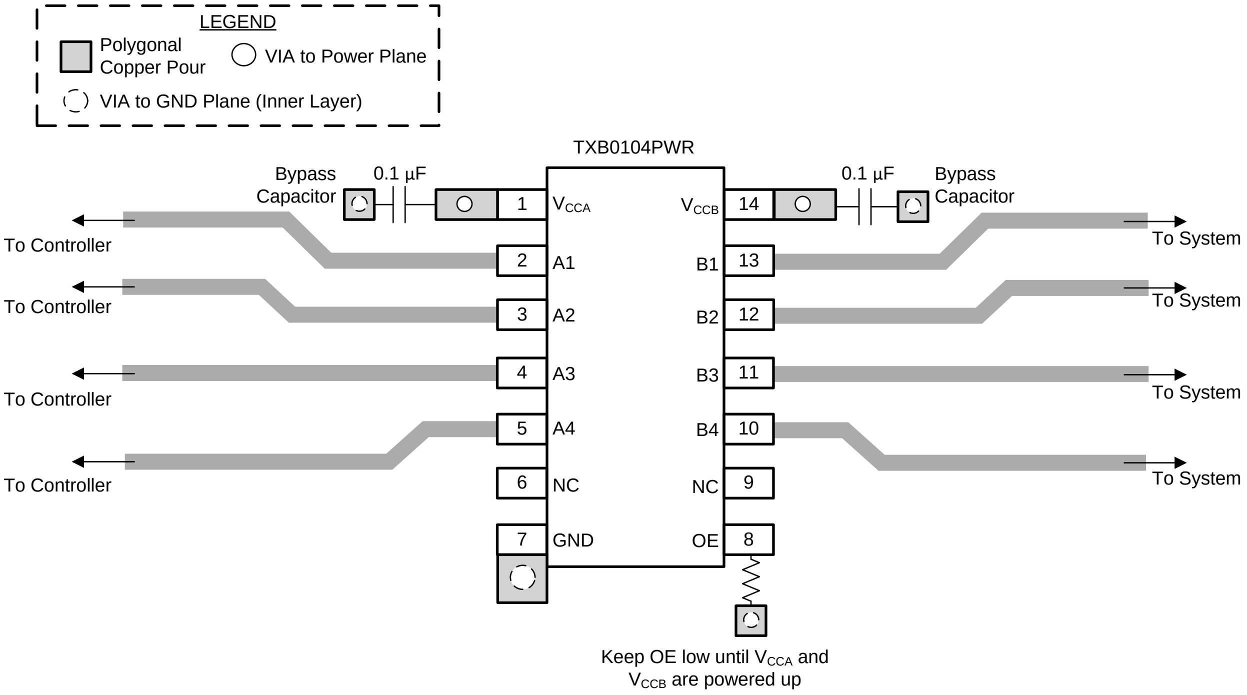
11 Layout

11.1 Layout Guidelines

To ensure reliability of the device, following common printed-circuit board layout guidelines is recommended.

- Bypass capacitors must be used on power supplies, and must be placed as close as possible to the V_{CCA}, V_{CCB} pin and GND pin.
- Short trace-lengths must be used to avoid excessive loading.
- PCB signal trace-lengths must be kept short enough so that the round-trip delay of any reflection is less than the one-shot duration, approximately 10 ns, ensuring that any reflection encounters low impedance at the source driver.

11.2 Layout Example



12 Device and Documentation Support

12.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.3 Trademarks

E2E is a trademark of Texas Instruments.
is a trademark of ~ Texas Instruments.
All other trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
HPA01164RUTR	ACTIVE	UQFN	RUT	12	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(2KR, 2KV)	Samples
TXB0104D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TXB0104	Samples
TXB0104DG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TXB0104	Samples
TXB0104DR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TXB0104	Samples
TXB0104DRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TXB0104	Samples
TXB0104PWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	YE04	Samples
TXB0104PWRG4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	YE04	Samples
TXB0104RGYR	ACTIVE	VQFN	RGY	14	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	YE04	Samples
TXB0104RGYRG4	ACTIVE	VQFN	RGY	14	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	YE04	Samples
TXB0104RUTR	ACTIVE	UQFN	RUT	12	3000	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	(2KR, 2KV)	Samples
TXB0104YZTR	ACTIVE	DSBGA	YZT	12	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	(2K, 2K7)	Samples
TXB0104ZXUR	ACTIVE	BGA MICROSTAR JUNIOR	ZXU	12	2500	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	YE04	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF TXB0104 :

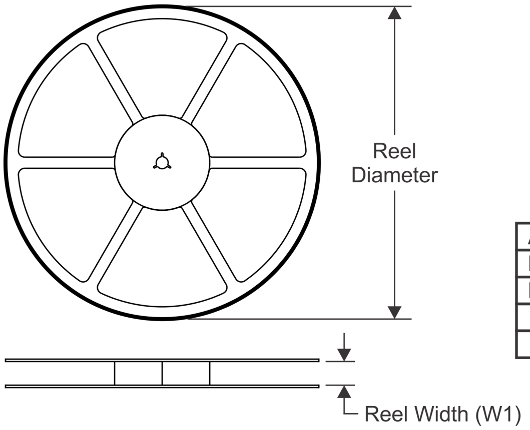
- Automotive: TXB0104-Q1

NOTE: Qualified Version Definitions:

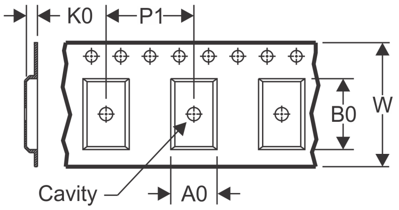
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

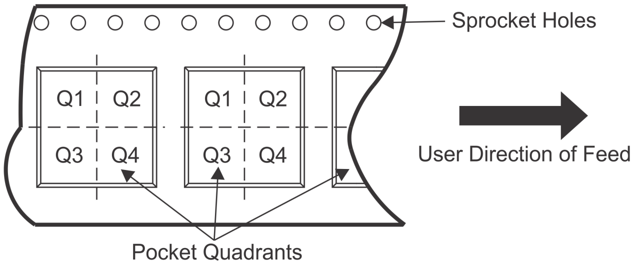


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

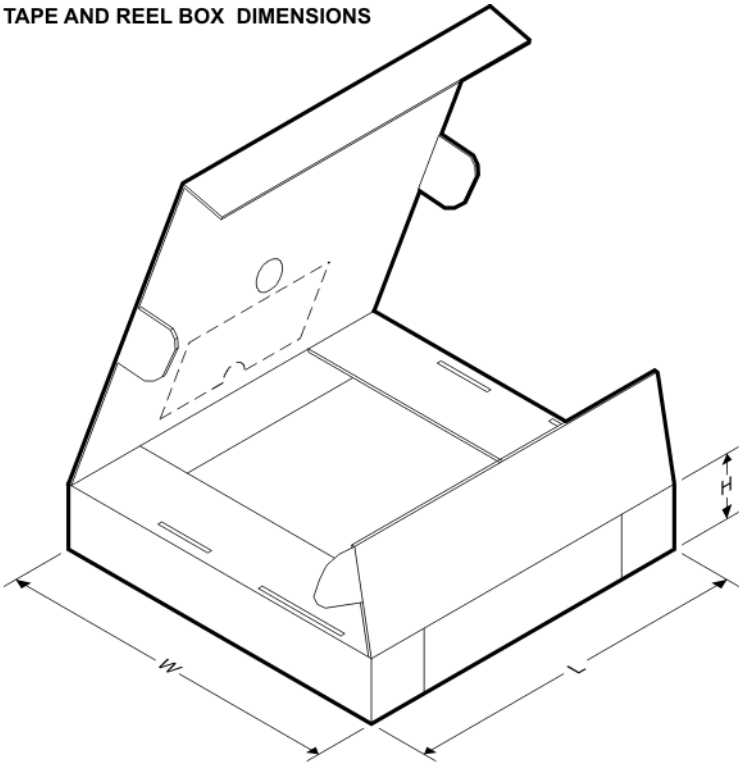
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TXB0104DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TXB0104PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TXB0104RGYR	VQFN	RGY	14	3000	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1
TXB0104RUTR	UQFN	RUT	12	3000	180.0	8.4	1.95	2.3	0.75	4.0	8.0	Q1
TXB0104RUTR	UQFN	RUT	12	3000	180.0	9.5	1.9	2.2	0.7	4.0	8.0	Q1
TXB0104YZTR	DSBGA	YZT	12	3000	180.0	8.4	1.49	1.99	0.75	4.0	8.0	Q2
TXB0104ZXUR	BGA MICROSTAR JUNIOR	ZXU	12	2500	330.0	8.4	2.3	2.8	1.0	4.0	8.0	Q2

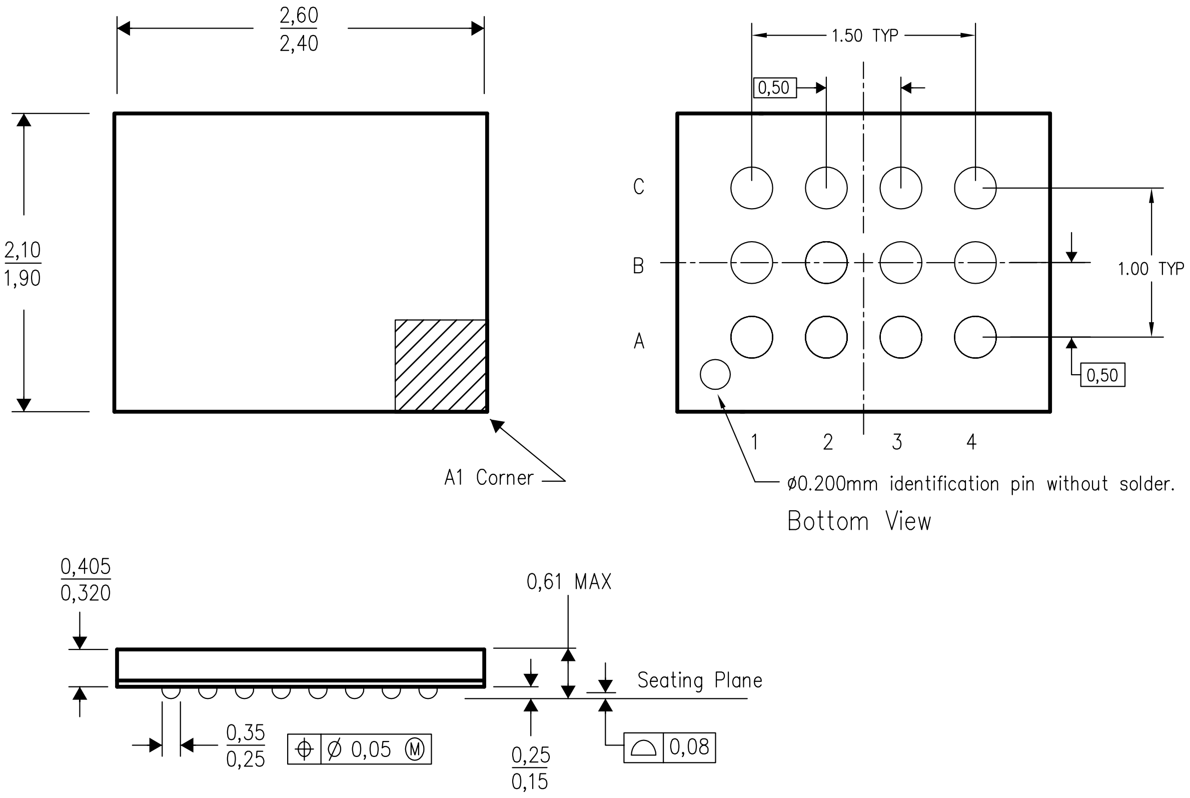
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TXB0104DR	SOIC	D	14	2500	367.0	367.0	38.0
TXB0104PWR	TSSOP	PW	14	2000	367.0	367.0	35.0
TXB0104RGYR	VQFN	RGY	14	3000	367.0	367.0	35.0
TXB0104RUTR	UQFN	RUT	12	3000	202.0	201.0	28.0
TXB0104RUTR	UQFN	RUT	12	3000	189.0	185.0	36.0
TXB0104YZTR	DSBGA	YZT	12	3000	182.0	182.0	20.0
TXB0104ZXUR	BGA MICROSTAR JUNIOR	ZXU	12	2500	336.6	336.6	28.6

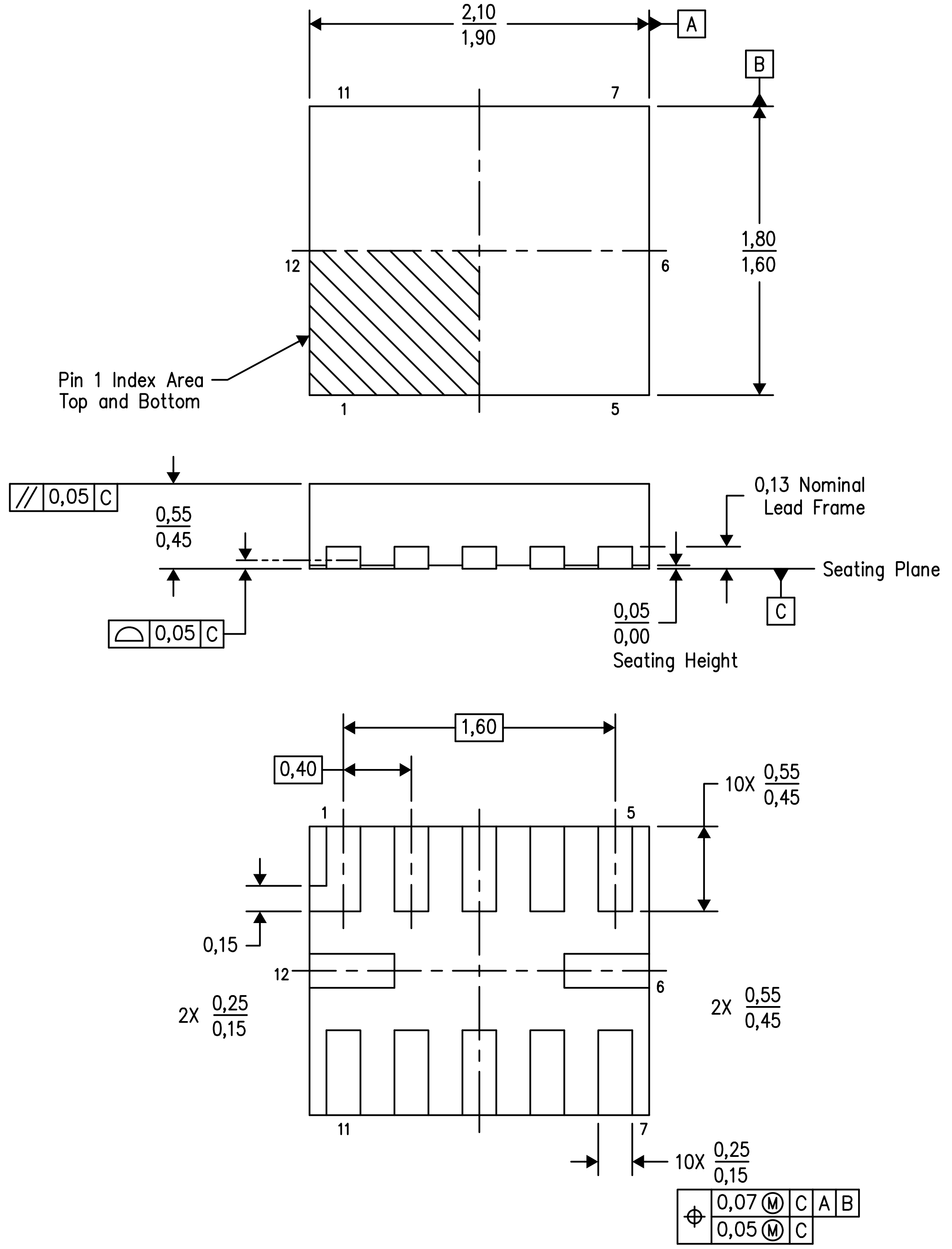
ZXU (S–PBGA–N12) PLASTIC BALL GRID ARRAY



4207009/B 06/05

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. This package is a lead–free solder ball design.

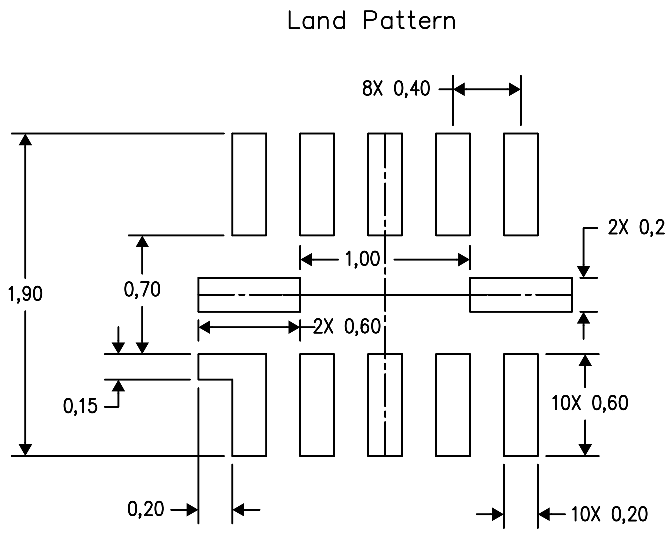
RUT (R–PUQFN–N12) PLASTIC QUAD FLATPACK NO–LEAD

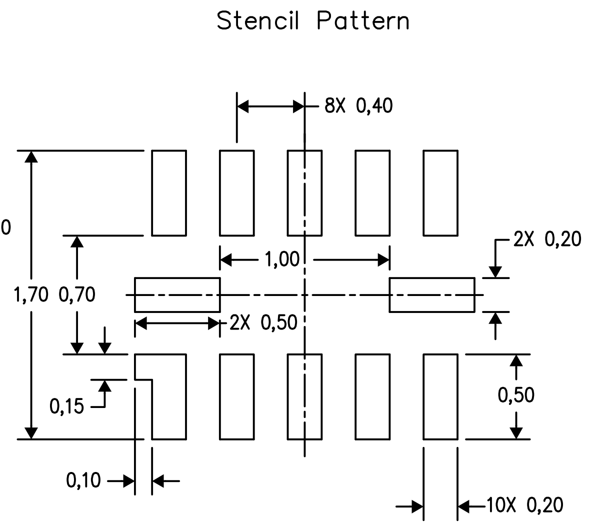


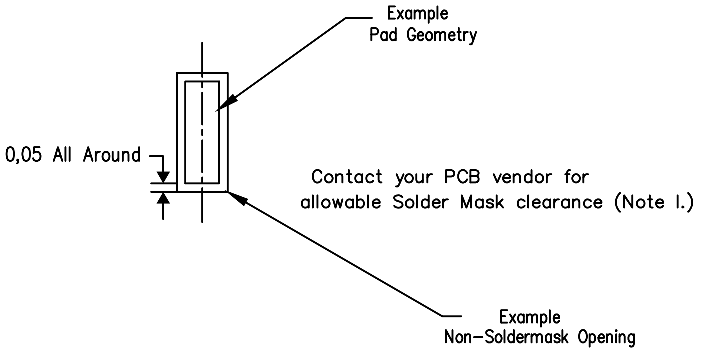
4210580/C 06/12

NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
- B. This drawing is subject to change without notice.
- C. QFN (Quad Flatpack No–Lead) package configuration.

RUT (R–PUQFN–N12) PLASTIC QUAD FLATPACK NO–LEAD



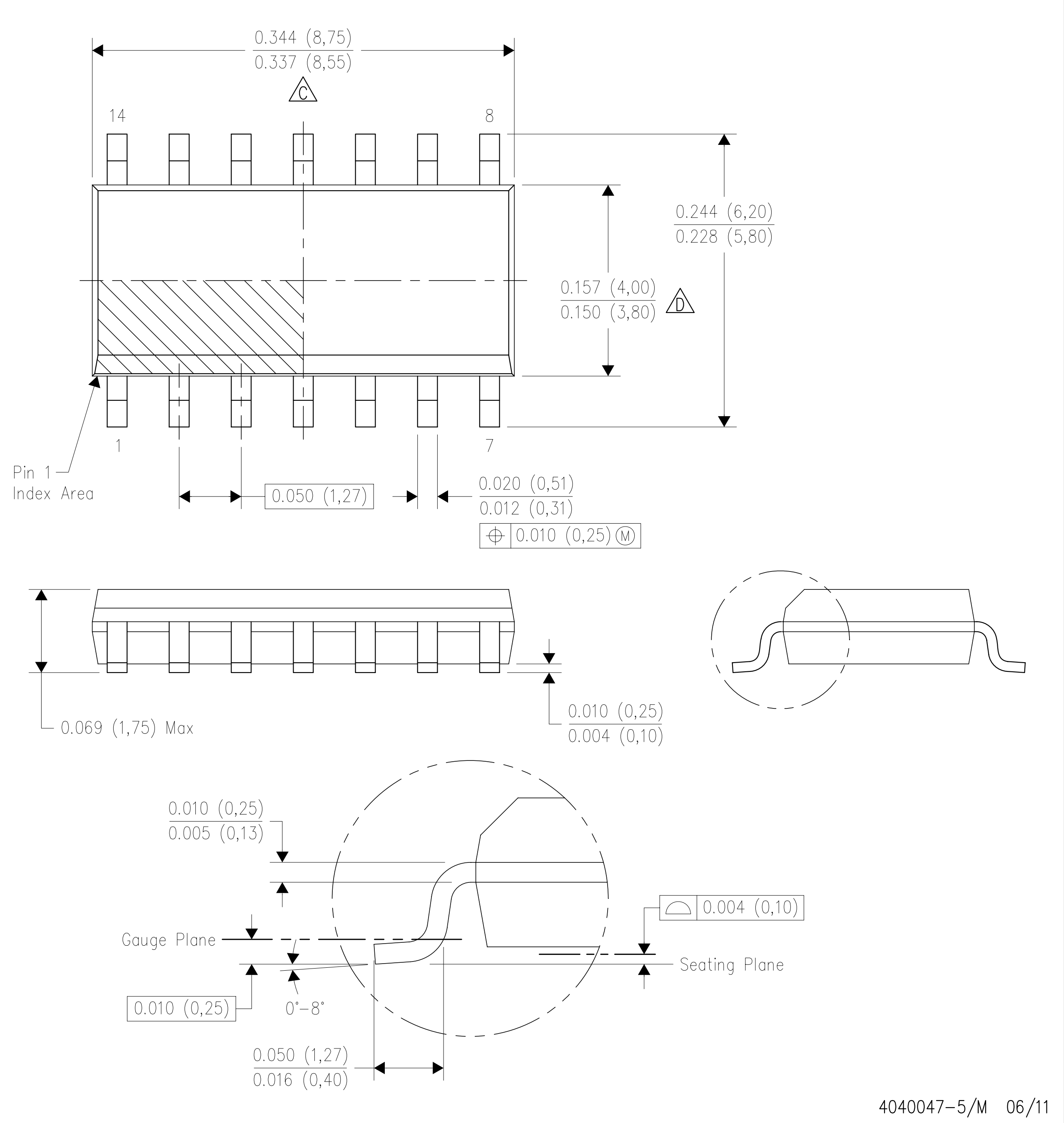




4212431/C 06/12

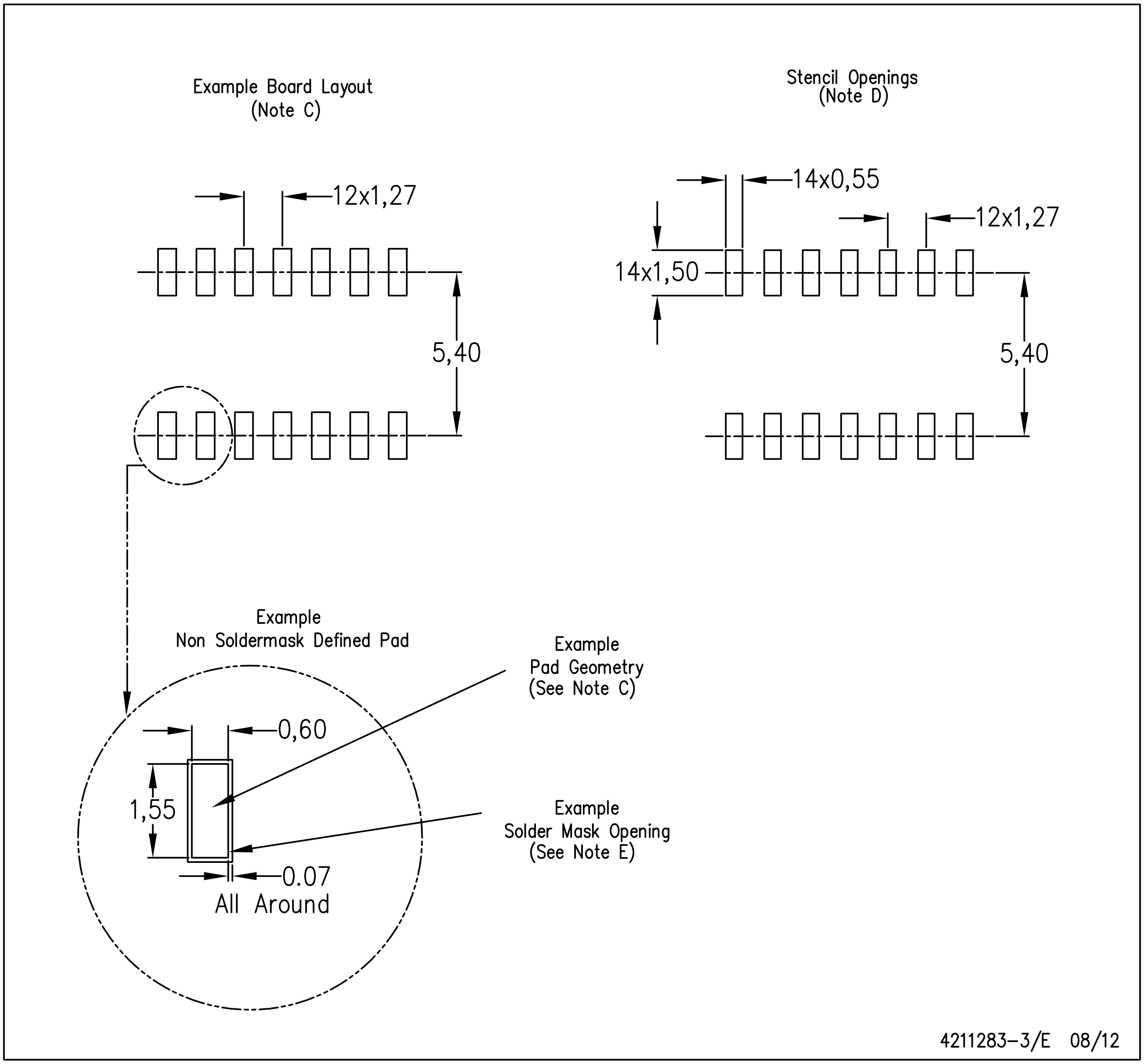
NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC–7351 is recommended for alternate designs.
- D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
- E. Maximum stencil thickness 0,1016 mm (4 mils). All linear dimensions are in millimeters.
- F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- G. Over–printing land for larger area ratio is not advised due to land width and bridging potential. Exersize extreme caution.
- H. Suggest stencils cut with lasers such as Fiber Laser that produce the greatest positional accuracy.
- I. Component placement force should be minimized to prevent excessive paste block deformation.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



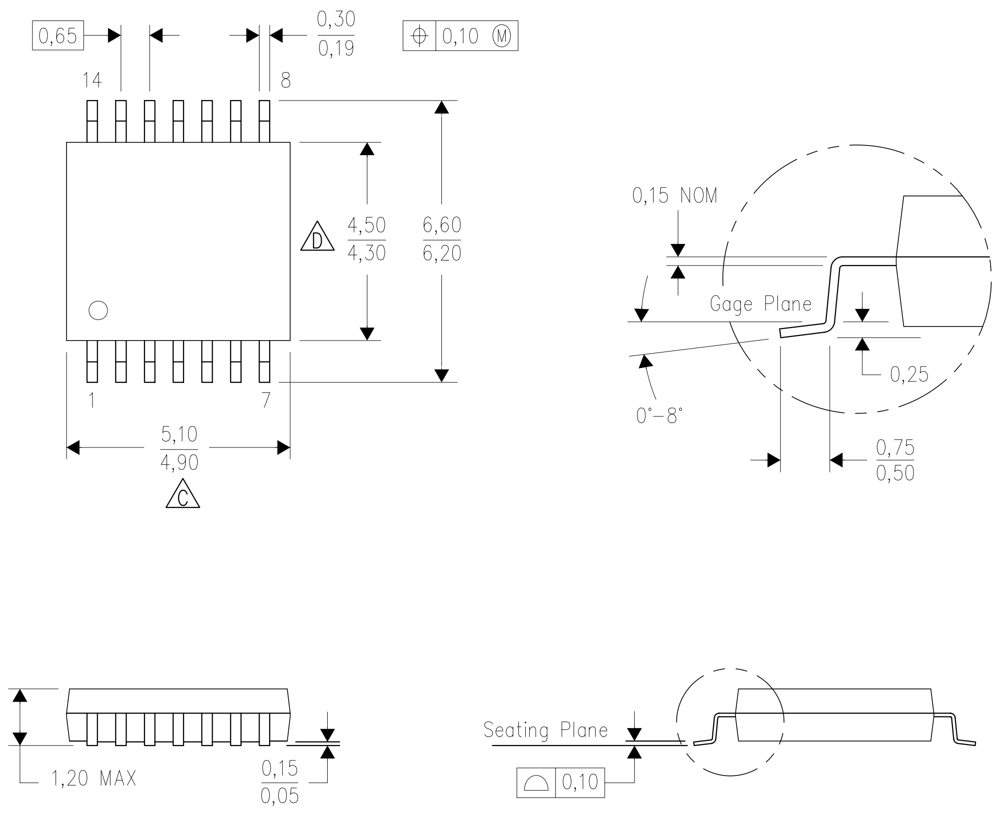
NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS–012 variation AB.

D (R-PDSO-G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G14) PLASTIC SMALL OUTLINE



4040064–3/G 02/11

NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
- E. Falls within JEDEC MO–153

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