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# FDC6401N

## Dual N-Channel 2.5V Specified PowerTrench<sup>®</sup> MOSFET

### General Description

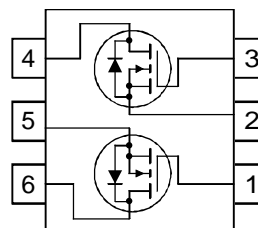
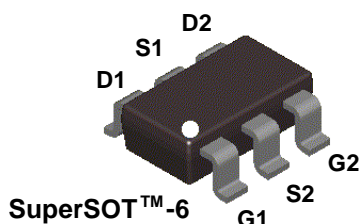
This Dual N-Channel MOSFET has been designed specifically to improve the overall efficiency of DC/DC converters using either synchronous or conventional switching PWM controllers. It has been optimized for low gate charge, low  $R_{DS(ON)}$  and fast switching speed.

### Applications

- DC/DC converter
- Battery Protection
- Power Management

### Features

- 3.0 A, 20 V.  $R_{DS(ON)} = 70\text{ m}\Omega$  @  $V_{GS} = 4.5\text{ V}$   
 $R_{DS(ON)} = 95\text{ m}\Omega$  @  $V_{GS} = 2.5\text{ V}$
- Low gate charge (3.3 nC)
- High performance trench technology for extremely low  $R_{DS(ON)}$
- High power and current handling capability



### Absolute Maximum Ratings T<sub>A</sub>=25°C unless otherwise noted

Symbol	Parameter	Ratings	Units
$V_{DSS}$	Drain-Source Voltage	20	V
$V_{GSS}$	Gate-Source Voltage	$\pm 12$	V
$I_D$	Drain Current – Continuous (Note 1a)	3.0	A
	– Pulsed	12	
$P_D$	Power Dissipation for Single Operation (Note 1a) (Note 1b) (Note 1c)	0.96	W
		0.9	
		0.7	
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to +150	°C

### Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1a)	130	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Note 1)	60	°C/W

### Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
.401	FDC6401N	7"	8mm	3000 units

## Electrical Characteristics

$T_A = 25^\circ\text{C}$  unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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### Off Characteristics

$BV_{DSS}$	Drain–Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	20			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$ , Referenced to $25^\circ\text{C}$		13		mV/ $^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 16\text{ V}, V_{GS} = 0\text{ V}$			1	$\mu\text{A}$
$I_{GSSF}$	Gate–Body Leakage, Forward	$V_{GS} = 12\text{ V}, V_{DS} = 0\text{ V}$			-100	nA
$I_{GSSR}$	Gate–Body Leakage, Reverse	$V_{GS} = -12\text{ V}, V_{DS} = 0\text{ V}$			100	nA

### On Characteristics (Note 2)

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	0.5	0.9	1.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$ , Referenced to $25^\circ\text{C}$		-3		mV/ $^\circ\text{C}$
$R_{DS(on)}$	Static Drain–Source On–Resistance	$V_{GS} = 4.5\text{ V}, I_D = 3.0\text{ A}$ $V_{GS} = 2.5\text{ V}, I_D = 2.5\text{ A}$ $V_{GS} = 4.5\text{ V}, I_D = 3.0\text{ A}, T_J = 125^\circ\text{C}$		50 66 71	70 95 106	m $\Omega$
$I_{D(on)}$	On–State Drain Current	$V_{GS} = 4.5\text{ V}, V_{DS} = 5\text{ V}$	12			A
$g_{FS}$	Forward Transconductance	$V_{DS} = 5\text{ V}, I_D = 3.0\text{ A}$		10		S

### Dynamic Characteristics

$C_{iss}$	Input Capacitance	$V_{DS} = 10\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$		324		pF
$C_{oss}$	Output Capacitance			82		pF
$C_{rss}$	Reverse Transfer Capacitance			42		pF

### Switching Characteristics (Note 2)

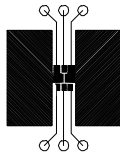
$t_{d(on)}$	Turn–On Delay Time	$V_{DD} = 10\text{ V}, I_D = 1\text{ A},$ $V_{GS} = 4.5\text{ V}, R_{GEN} = 6\ \Omega$		5	10	ns
$t_r$	Turn–On Rise Time			7	14	ns
$t_{d(off)}$	Turn–Off Delay Time			13	23	ns
$t_f$	Turn–Off Fall Time			1.6	3	ns
$Q_g$	Total Gate Charge	$V_{DS} = 10\text{ V}, I_D = 3.0\text{ A},$ $V_{GS} = 4.5\text{ V}$		3.3	4.6	nC
$Q_{gs}$	Gate–Source Charge			0.95		nC
$Q_{gd}$	Gate–Drain Charge			0.7		nC

### Drain–Source Diode Characteristics and Maximum Ratings

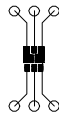
$I_S$	Maximum Continuous Drain–Source Diode Forward Current			0.8		A
$V_{SD}$	Drain–Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 0.8\text{ A}$ (Note 2)		0.7	1.2	V

#### Notes:

1.  $R_{\theta JA}$  is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.



a) 130  $^\circ\text{C}/\text{W}$  when mounted on a 0.125 in<sup>2</sup> pad of 2 oz. copper.



b) 140  $^\circ\text{C}/\text{W}$  when mounted on a .004 in<sup>2</sup> pad of 2 oz copper



c) 180  $^\circ\text{C}/\text{W}$  when mounted on a minimum pad.

Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width < 300 $\mu\text{s}$ , Duty Cycle < 2.0%

## Typical Characteristics

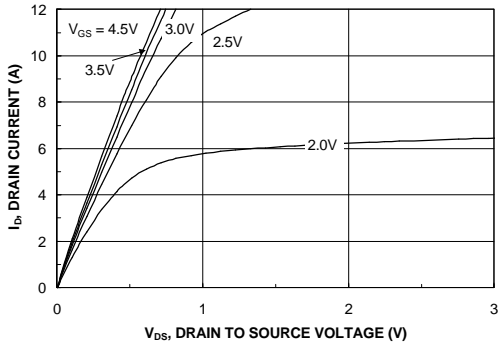


Figure 1. On-Region Characteristics.

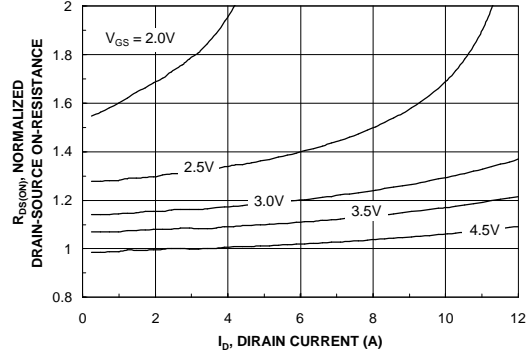


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

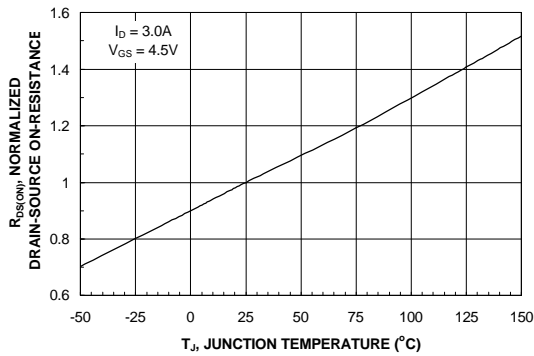


Figure 3. On-Resistance Variation with Temperature.

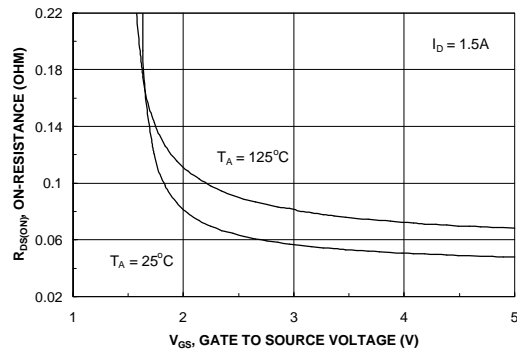


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

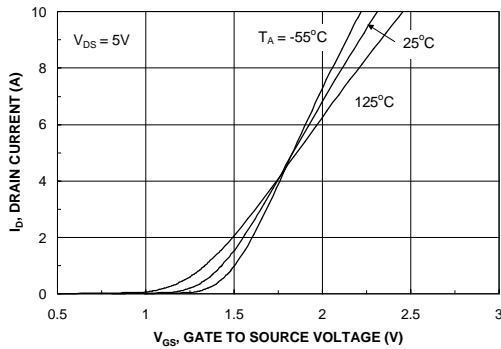


Figure 5. Transfer Characteristics.

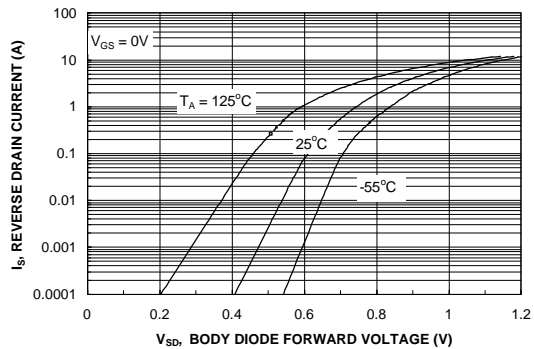
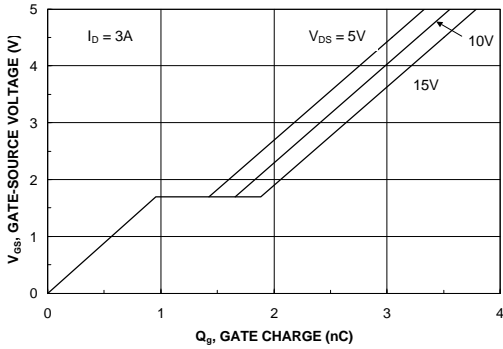
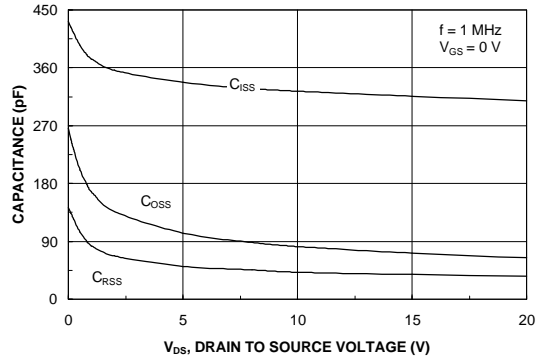


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

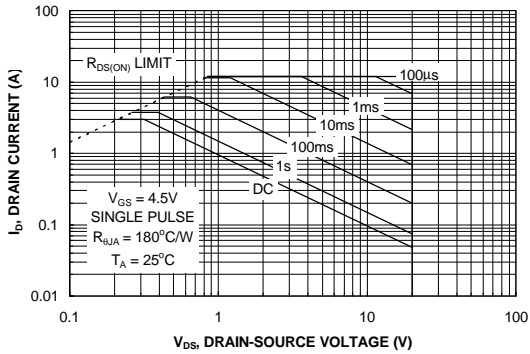
## Typical Characteristics



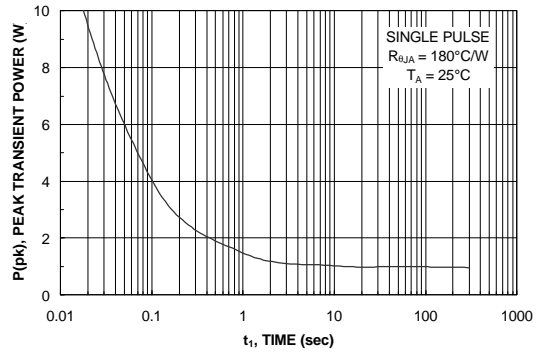
**Figure 7. Gate Charge Characteristics.**



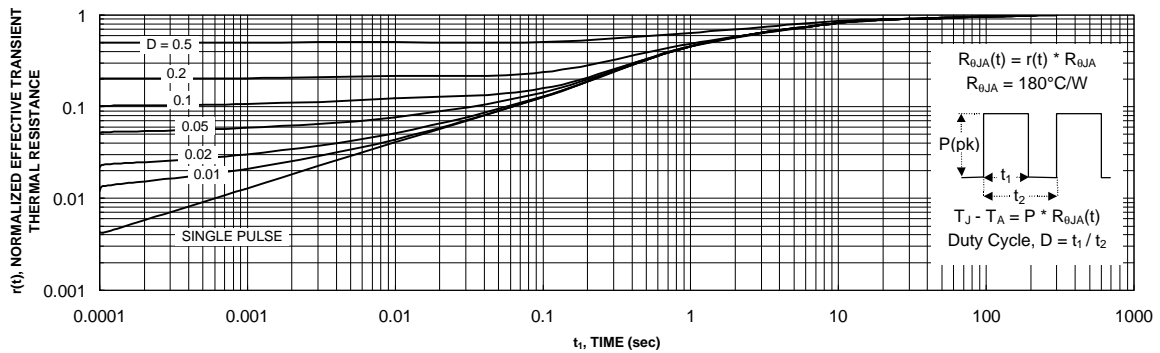
**Figure 8. Capacitance Characteristics.**



**Figure 9. Maximum Safe Operating Area.**



**Figure 10. Single Pulse Maximum Power Dissipation.**



**Figure 11. Transient Thermal Response Curve.**

Thermal characterization performed using the conditions described in Note 1c.  
Transient thermal response will change depending on the circuit board design.

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