

GigaDevice Semiconductor Inc.

GD32F107xx
ARM[®] Cortex[™]-M3 32-bit MCU

Datasheet

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1 General description

The GD32F107xx device belongs to the connectivity line of GD32 MCU Family. It is a 32-bit general-purpose microcontroller based on the ARM[®] Cortex[™]-M3 RISC core with enhanced connectivity performance and best ratio in terms of processing power, reduced power consumption and peripheral set. The Cortex[™]-M3 is a next generation processor core which is tightly coupled with a Nested Vectored Interrupt Controller (NVIC), SysTick timer and advanced debug support.

The GD32F107xx device incorporates the ARM[®] Cortex[™]-M3 32-bit processor core operating at 108 MHz frequency with Flash accesses zero wait states to obtain maximum efficiency. It provides up to 1 MB on-chip Flash memory and 96 KB SRAM memory. An extensive range of enhanced I/Os and peripherals connected to two APB buses. The devices offer up to three 12-bit ADCs, up to two 12-bit DACs, up to ten general-purpose 16-bit timers, two basic timers plus two PWM advanced-control timer, as well as standard and advanced communication interfaces: up to three SPIs, two I²Cs, three USARTs, two UARTs, two I²Ss, two CANs, an USB OTG FS and an Ethernet MAC.

The device operates from a 2.6 to 3.6 V power supply and available in –40 to +85 °C temperature range. Several power saving modes provide the flexibility for maximum optimization between wakeup latency and power consumption, an especially important consideration in low power applications.

The above features make the GD32F107xx devices suitable for a wide range of interconnection applications, especially in areas such as industrial control, motor drives, power monitor and alarm systems, consumer and handheld equipment, POS, vehicle GPS, LED display and so on.

2 Device overview

2.1 Device information

Table 1. GD32F107xx devices features and peripheral list

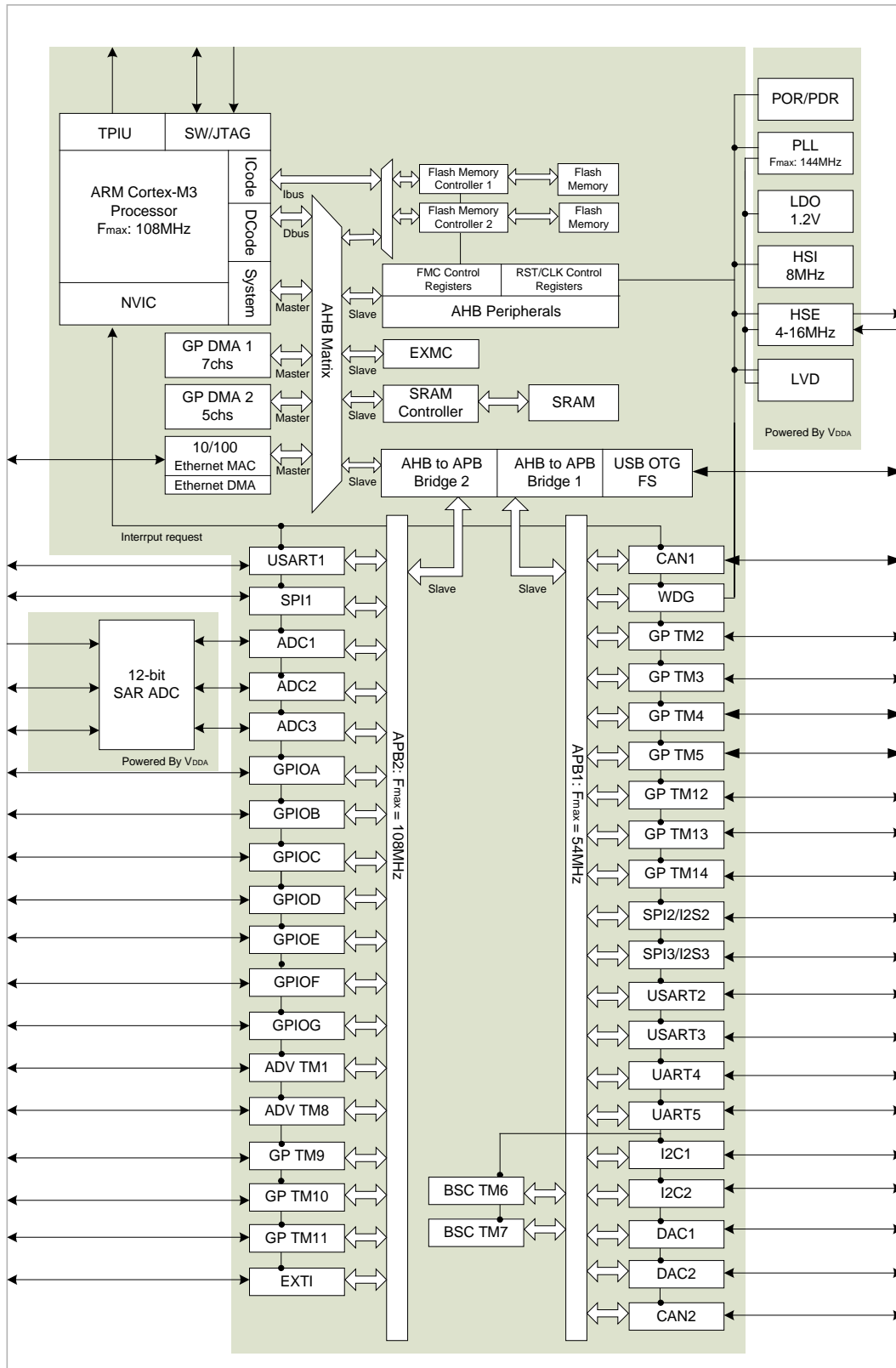
| Part Number | | GD32F107xx | | | | | | | |
|--------------|--------------|------------|-----|-----|-----|-----|---------|-----|-----|
| | | RB | RC | RD | RE | RF | RG | VB | VC |
| Flash (KB) | | 128 | 256 | 384 | 512 | 768 | 1024 | 128 | 256 |
| SRAM (KB) | | 96 | 96 | 96 | 96 | 96 | 96 | 96 | 96 |
| Timers | GPTM | 4 | 4 | 4 | 4 | 10 | 10 | 4 | 4 |
| | Advanced TM | 1 | 1 | 2 | 2 | 2 | 2 | 1 | 1 |
| | SysTick | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | Basic TM | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 |
| | Watchdog | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 |
| | RTC | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| Connectivity | U(S)ART | 5 | 5 | 5 | 5 | 5 | 5 | 5 | 5 |
| | I2C | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 |
| | SPI | 3 | 3 | 3 | 3 | 3 | 3 | 3 | 3 |
| | I2S | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 |
| | CAN 2.0B | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 |
| | USB OTG FS | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | Ethernet MAC | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| GPIO | | 51 | 51 | 51 | 51 | 51 | 51 | 80 | 80 |
| EXMC | | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| EXTI | | 16 | 16 | 16 | 16 | 16 | 16 | 16 | 16 |
| ADC | Units | 3 | 3 | 3 | 3 | 3 | 3 | 3 | 3 |
| | Channels | 16 | 16 | 16 | 16 | 16 | 16 | 16 | 16 |
| DAC | | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 |
| Package | | LQFP64 | | | | | LQFP100 | | |

Table 1. GD32F107xx devices features and peripheral list (continued)

| Part Number | | GD32F107xx | | | | | | | | |
|--------------|--------------|------------|-----|-----|------|---------|-----|-----|-----|------|
| | | VD | VE | VF | VG | ZC | ZD | ZE | ZF | ZG |
| Flash (KB) | | 384 | 512 | 768 | 1024 | 256 | 384 | 512 | 768 | 1024 |
| SRAM (KB) | | 96 | 96 | 96 | 96 | 96 | 96 | 96 | 96 | 96 |
| Timers | GPTM | 4 | 4 | 10 | 10 | 4 | 4 | 4 | 10 | 10 |
| | Advanced TM | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 |
| | SysTick | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | Basic TM | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 |
| | Watchdog | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 |
| | RTC | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| Connectivity | U(S)ART | 5 | 5 | 5 | 5 | 5 | 5 | 5 | 5 | 5 |
| | I2C | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 |
| | SPI | 3 | 3 | 3 | 3 | 3 | 3 | 3 | 3 | 3 |
| | I2S | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 |
| | CAN 2.0B | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 |
| | USB OTG FS | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | Ethernet MAC | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| GPIO | | 80 | 80 | 80 | 80 | 112 | 112 | 112 | 112 | 112 |
| EXMC | | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| EXTI | | 16 | 16 | 16 | 16 | 16 | 16 | 16 | 16 | 16 |
| ADC | Units | 3 | 3 | 3 | 3 | 3 | 3 | 3 | 3 | 3 |
| | Channels | 16 | 16 | 16 | 16 | 21 | 21 | 21 | 21 | 21 |
| DAC | | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 |
| Package | | LQFP100 | | | | LQFP144 | | | | |

2.2 Block diagram

Figure 1. GD32F107xx block diagram



2.3 Pinouts and pin assignment

Figure 2. GD32F107Zx LQFP144 pinouts

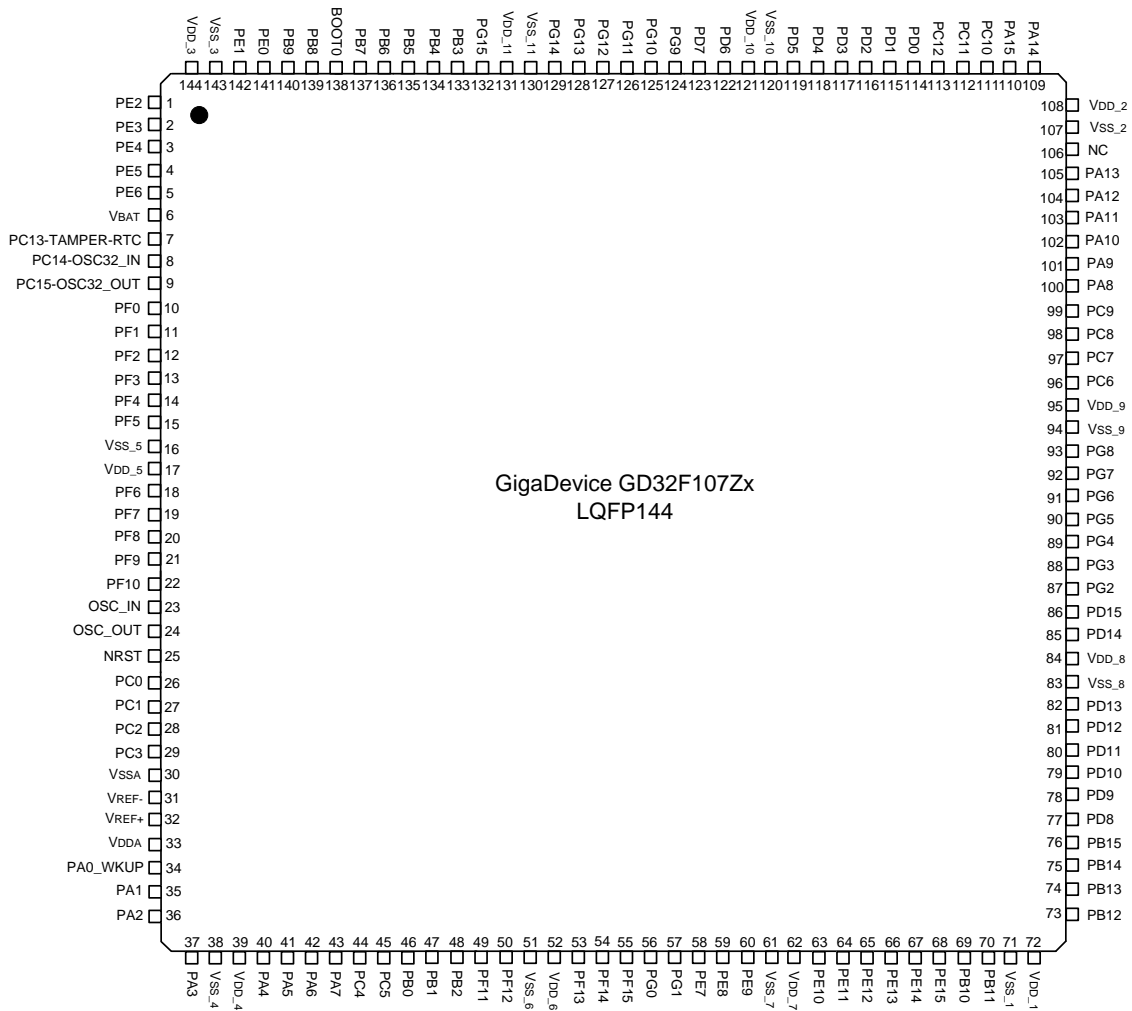


Figure 3. GD32F107Vx LQFP100 pinouts

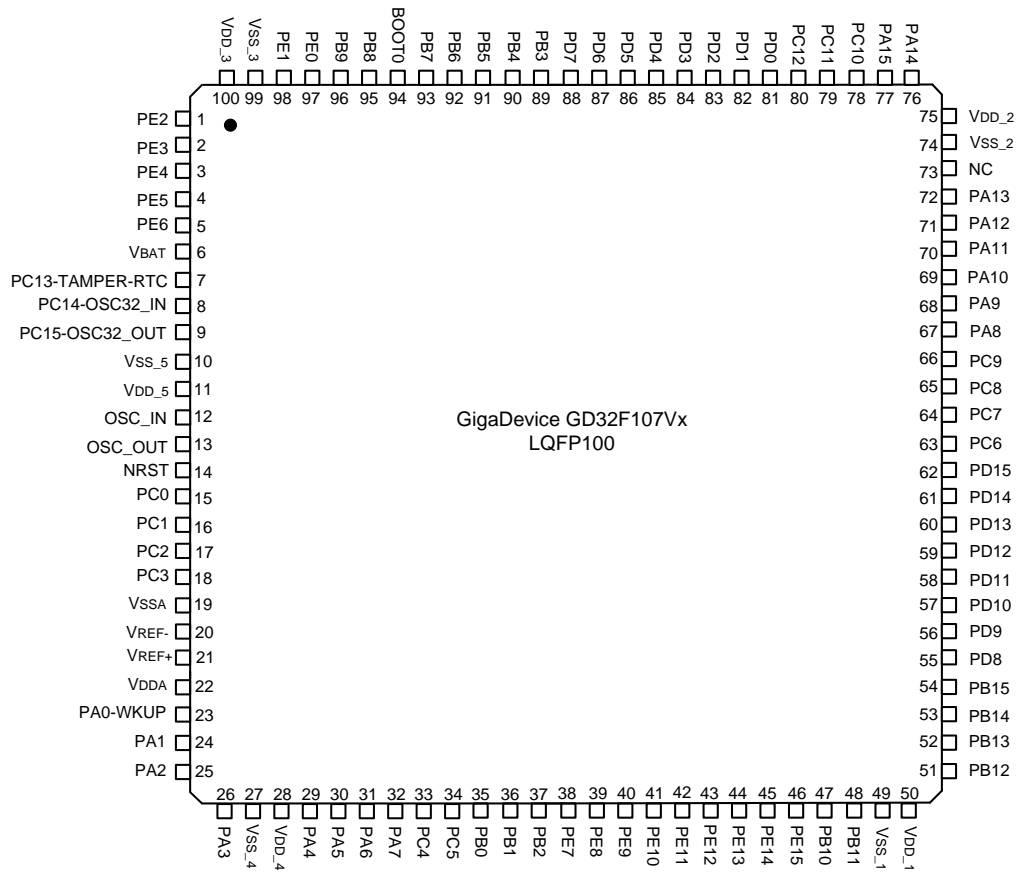
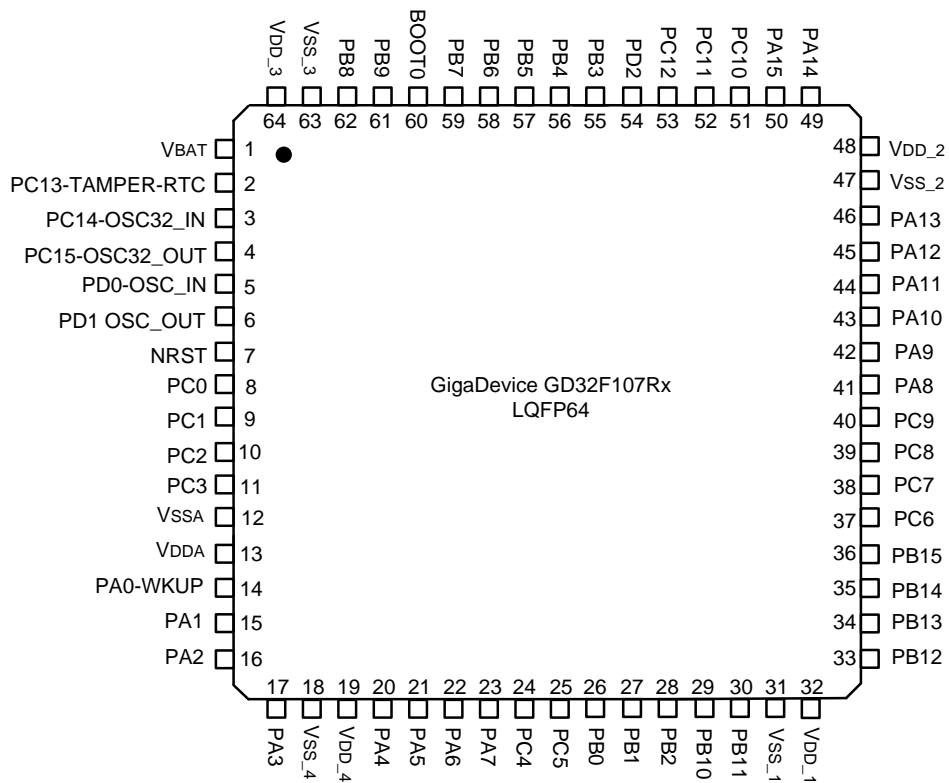
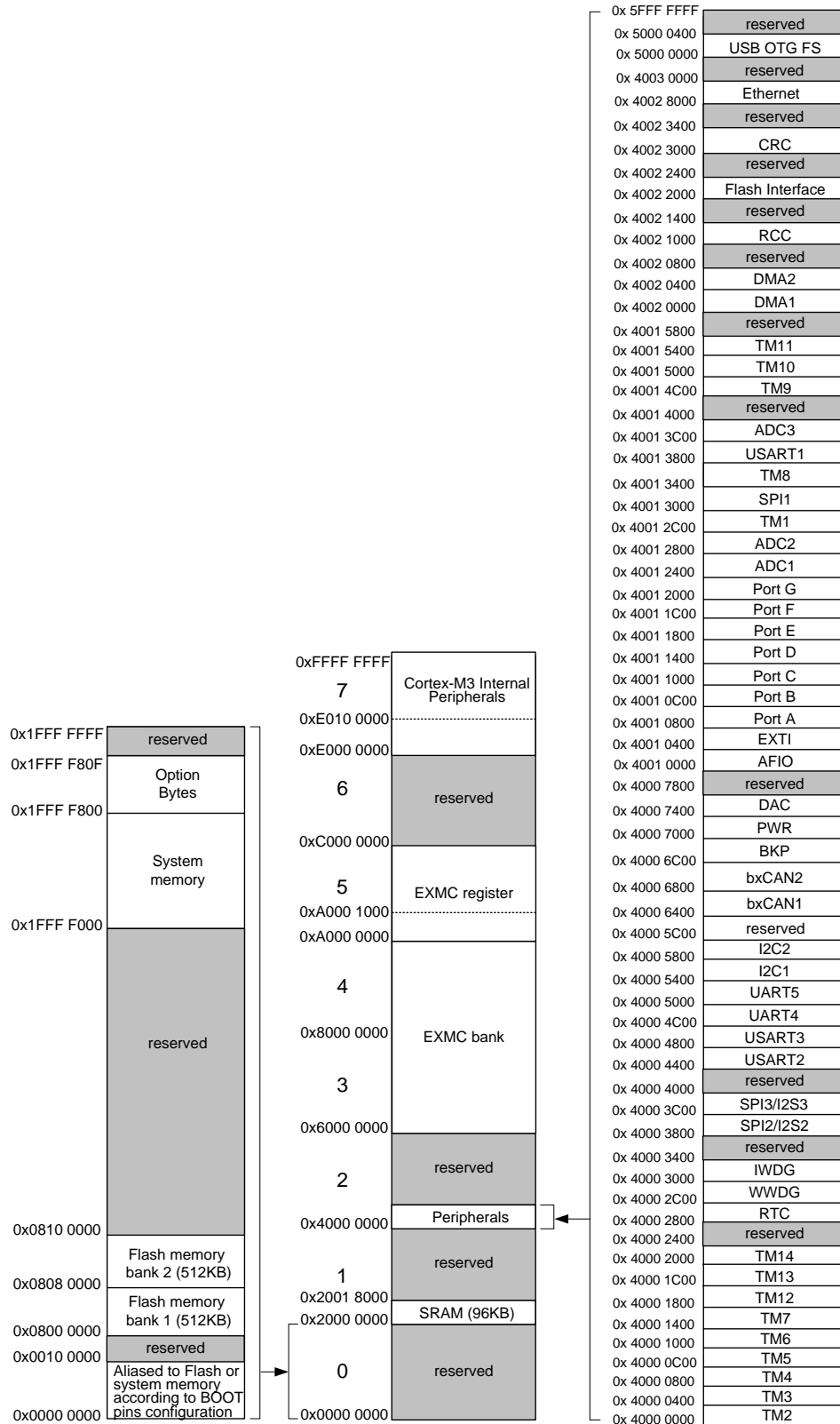


Figure 4. GD32F107Rx LQFP64 pinouts



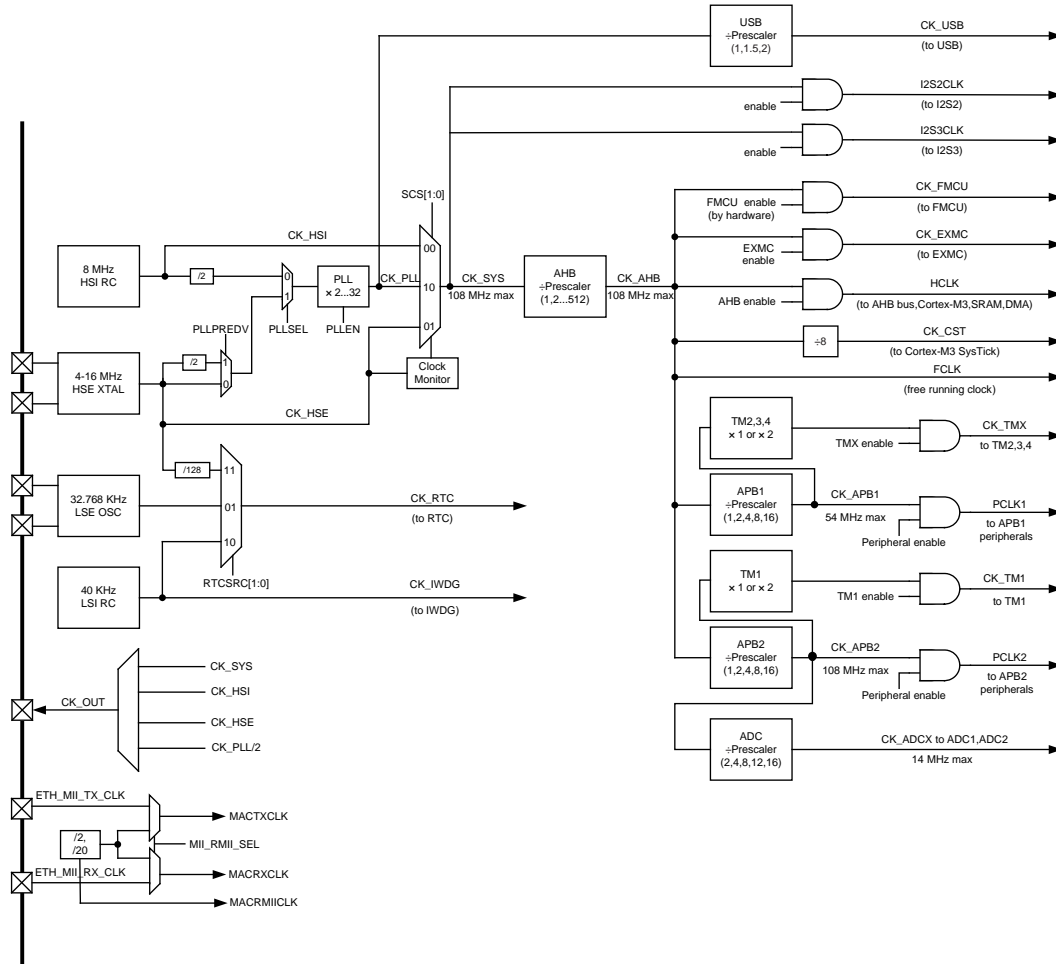
2.4 Memory map

Figure 5. GD32F107xx memory map



2.5 Clock tree

Figure 6. GD32F107xx clock tree



Legend:

- HSE = High speed external clock
- HSI = High speed internal clock
- LSE = Low speed external clock
- LSI = Low speed internal clock

2.6 Pin definitions

Table 2. GD32F107xx pin definitions

| Pin Name | Pins | | | Pin Type ⁽¹⁾ | I/O ⁽²⁾ Level | Functions description |
|---------------------|---------|---------|--------|-------------------------|--------------------------|---|
| | LQFP144 | LQFP100 | LQFP64 | | | |
| PE2 | 1 | 1 | - | I/O | 5VT | Default: PE2 Alternate: TRACECK, EXMC_A23 |
| PE3 | 2 | 2 | - | I/O | 5VT | Default: PE3 Alternate: TRACED0, EXMC_A19 |
| PE4 | 3 | 3 | - | I/O | 5VT | Default: PE4 Alternate: TRACED1, EXMC_A20 |
| PE5 | 4 | 4 | - | I/O | 5VT | Default: PE5 Alternate: TRACED2, EXMC_A21 Remap: TM9_CH1 ⁽⁴⁾ |
| PE6 | 5 | 5 | - | I/O | 5VT | Default: PE6 Alternate: TRACED3, EXMC_A22 Remap: TM9_CH2 ⁽⁴⁾ |
| V _{BAT} | 6 | 6 | 1 | P | | Default: V _{BAT} |
| PC13-TAMPE R-RTC | 7 | 7 | 2 | I/O | | Default: PC13 Alternate: TAMPER-RTC |
| PC14-OSC32 _IN | 8 | 8 | 3 | I/O | | Default: PC14 Alternate: OSC32_IN |
| PC15- OSC32_OUT | 9 | 9 | 4 | I/O | | Default: PC15 Alternate: OSC32_OUT |
| PF0 | 10 | - | - | I/O | 5VT | Default: PF0 ⁽³⁾ Alternate: EXMC_A0 ⁽³⁾ |
| PF1 | 11 | - | - | I/O | 5VT | Default: PF1 ⁽³⁾ Alternate: EXMC_A1 ⁽³⁾ |
| PF2 | 12 | - | - | I/O | 5VT | Default: PF2 ⁽³⁾ Alternate: EXMC_A2 ⁽³⁾ |
| PF3 | 13 | - | - | I/O | 5VT | Default: PF3 ⁽³⁾ Alternate: EXMC_A3 ⁽³⁾ |
| PF4 | 14 | - | - | I/O | 5VT | Default: PF4 ⁽³⁾ Alternate: EXMC_A4 ⁽³⁾ |
| PF5 | 15 | - | - | I/O | 5VT | Default: PF5 ⁽³⁾ Alternate: EXMC_A5 ⁽³⁾ |
| V _{SS_5} | 16 | 10 | - | P | | Default: V _{SS_5} |
| V _{DD_5} | 17 | 11 | - | P | | Default: V _{DD_5} |
| PF6 | 18 | - | - | I/O | | Default: PF6 ⁽³⁾ Alternate: ADC3_IN4 ⁽³⁾ , EXMC_NIORD ⁽³⁾ Remap: TM10_CH1 ⁽⁴⁾ |
| PF7 | 19 | - | - | I/O | | Default: PF7 ⁽³⁾ Alternate: ADC3_IN5 ⁽³⁾ , EXMC_NREG ⁽³⁾ |

| Pin Name | Pins | | | Pin Type ⁽¹⁾ | I/O ⁽²⁾ Level | Functions description |
|-------------------|---------|---------|--------|-------------------------|--------------------------|---|
| | LQFP144 | LQFP100 | LQFP64 | | | |
| | | | | | | Remap: TM11_CH1 ⁽⁴⁾ |
| PF8 | 20 | - | - | I/O | | Default: PF8 ⁽³⁾ Alternate: ADC3_IN6 ⁽³⁾ , EXMC_NIOWR ⁽³⁾ Remap: TM13_CH1 ⁽⁴⁾ |
| PF9 | 21 | - | - | I/O | | Default: PF9 ⁽³⁾ Alternate: ADC3_IN7 ⁽³⁾ , EXMC_CD ⁽³⁾ Remap: TM14_CH1 ⁽⁴⁾ |
| PF10 | 22 | - | - | I/O | | Default: PF10 ⁽³⁾ Alternate: ADC3_IN8 ⁽³⁾ , EXMC_INTR ⁽³⁾ |
| OSC_IN | 23 | 12 | 5 | I | | Default: OSC_IN Remap: PD0 ⁽⁴⁾ |
| OSC_OUT | 24 | 13 | 6 | O | | Default: OSC_OUT Remap: PD1 ⁽⁴⁾ |
| NRST | 25 | 14 | 7 | I/O | | Default: NRST |
| PC0 | 26 | 15 | 8 | I/O | | Default: PC0 Alternate: ADC_IN10 |
| PC1 | 27 | 16 | 9 | I/O | | Default: PC1 Alternate: ADC_IN11, ETH_MII_MDC, ETH_RMII_MDC |
| PC2 | 28 | 17 | 10 | I/O | | Default: PC2 Alternate: ADC_IN12, ETH_MII_TXD2 |
| PC3 | 29 | 18 | 11 | I/O | | Default: PC3 Alternate: ADC_IN13, ETH_MII_TX_CLK |
| V _{SSA} | 30 | 19 | 12 | P | | Default: V _{SSA} |
| V _{REF-} | 31 | 20 | - | P | | Default: V _{REF-} |
| V _{REF+} | 32 | 21 | - | P | | Default: V _{REF+} |
| V _{DDA} | 33 | 22 | 13 | P | | Default: V _{DDA} |
| PA0-WKUP | 34 | 23 | 14 | I/O | | Default: PA0 Alternate: WKUP, USART2_CTS, ADC_IN0, TM2_CH1_ETR, TM5_CH1 ⁽³⁾ , TM8_ETR ⁽³⁾ , ETH_MII_CRS_WKUP |
| PA1 | 35 | 24 | 15 | I/O | | Default: PA1 Alternate: USART2_RTS, ADC_IN1, TM2_CH2, TM5_CH2 ⁽³⁾ , ETH_MII_RX_CLK, ETH_RMII_REF_CLK |
| PA2 | 36 | 25 | 16 | I/O | | Default: PA2 Alternate: USART2_TX, ADC_IN2, TM2_CH3, TM5_CH3 ⁽³⁾ , TM9_CH1 ⁽⁴⁾ , ETH_MII_MDIO, ETH_RMII_MDIO |
| PA3 | 37 | 26 | 17 | I/O | | Default: PA3 Alternate: USART2_RX, ADC_IN3, TM2_CH4, TM5_CH4 ⁽³⁾ , TM9_CH2 ⁽⁴⁾ , ETH_MII_COL |
| V _{SS_4} | 38 | 27 | 18 | P | | Default: V _{SS_4} |
| V _{DD_4} | 39 | 28 | 19 | P | | Default: V _{DD_4} |
| PA4 | 40 | 29 | 20 | I/O | | Default: PA4 Alternate: SPI1_NSS, USART2_CK, ADC12_IN4; DAC_OUT1 ⁽³⁾ |

| Pin Name | Pins | | | Pin Type ⁽¹⁾ | I/O ⁽²⁾ Level | Functions description |
|-------------------|---------|---------|--------|-------------------------|--------------------------|--|
| | LQFP144 | LQFP100 | LQFP64 | | | |
| | | | | | | Remap:SPI3_NSS ⁽³⁾ , I2S3_WS ⁽³⁾ |
| PA5 | 41 | 30 | 21 | I/O | | Default: PA5 Alternate: SPI1_SCK, ADC12_IN5, DAC_OUT2 ⁽³⁾ |
| PA6 | 42 | 31 | 22 | I/O | | Default: PA6 Alternate: SPI1_MISO, ADC12_IN6, TM3_CH1, TM8_BKIN ⁽³⁾ , TM13_CH1 ⁽⁴⁾ Remap: TM1_BKIN |
| PA7 | 43 | 32 | 23 | I/O | | Default: PA7 Alternate: SPI1_MOSI, ADC12_IN7, TM3_CH2, TM8_CH1N ⁽³⁾ , TM14_CH1 ⁽⁴⁾ , ETH_MII_RX_DV, ETH_RMII_CRD_DV Remap: TM1_CH1N |
| PC4 | 44 | 33 | 24 | I/O | | Default: PC4 Alternate: ADC12_IN14, ETH_MII_RXD0, ETH_RMII_RXD0 |
| PC5 | 45 | 34 | 25 | I/O | | Default: PC5 Alternate: ADC12_IN15, ETH_MII_RXD1, ETH_RMII_RXD1 |
| PB0 | 46 | 35 | 26 | I/O | | Default: PB0 Alternate: ADC12_IN8, TM3_CH3, TM8_CH2N ⁽³⁾ , ETH_MII_RXD2 Remap: TM1_CH2N |
| PB1 | 47 | 36 | 27 | I/O | | Default: PB1 Alternate: ADC12_IN9, TM3_CH4, TM8_CH3N ⁽³⁾ , ETH_MII_RXD3 Remap: TM1_CH3N |
| PB2 | 48 | 37 | 28 | I/O | 5VT | Default: PB2/BOOT1 |
| PF11 | 49 | - | - | I/O | 5VT | Default: PF11 ⁽³⁾ Alternate: EXMC_NIOS16 ⁽³⁾ |
| PF12 | 50 | - | - | I/O | 5VT | Default: PF12 ⁽³⁾ Alternate: EXMC_A6 ⁽³⁾ |
| V _{SS_6} | 51 | - | - | P | | Default: V _{SS_6} |
| V _{DD_6} | 52 | - | - | P | | Default: V _{DD_6} |
| PF13 | 53 | - | - | I/O | 5VT | Default: PF13 ⁽³⁾ Alternate: EXMC_A7 ⁽³⁾ |
| PF14 | 54 | - | - | I/O | 5VT | Default: PF14 ⁽³⁾ Alternate: EXMC_A8 ⁽³⁾ |
| PF15 | 55 | - | - | I/O | 5VT | Default: PF15 ⁽³⁾ Alternate: EXMC_A9 ⁽³⁾ |
| PG0 | 56 | - | - | I/O | 5VT | Default: PG0 ⁽³⁾ Alternate: EXMC_A10 ⁽³⁾ |
| PG1 | 57 | - | - | I/O | 5VT | Default: PG1 ⁽³⁾ Alternate: EXMC_A11 ⁽³⁾ |
| PE7 | 58 | 38 | - | I/O | 5VT | Default: PE7 Alternate: EXMC_D4 Remap: TM1_ETR |
| PE8 | 59 | 39 | - | I/O | 5VT | Default: PE8 Alternate: EXMC_D5 |

| Pin Name | Pins | | | Pin Type ⁽¹⁾ | I/O ⁽²⁾ Level | Functions description |
|-------------------|---------|---------|--------|-------------------------|--------------------------|--|
| | LQFP144 | LQFP100 | LQFP64 | | | |
| | | | | | | Remap: TM1_CH1N |
| PE9 | 60 | 40 | - | I/O | 5VT | Default: PE9 Alternate: EXMC_D6 Remap: TM1_CH1 |
| V _{SS_7} | 61 | - | - | P | | Default: V _{SS_7} |
| V _{DD_7} | 62 | - | - | P | | Default: V _{DD_7} |
| PE10 | 63 | 41 | - | I/O | 5VT | Default: PE10 Alternate: EXMC_D7 Remap: TM1_CH2N |
| PE11 | 64 | 42 | - | I/O | 5VT | Default: PE11 Alternate: EXMC_D8 Remap: TM1_CH2 |
| PE12 | 65 | 43 | - | I/O | 5VT | Default: PE12 Alternate: EXMC_D9 Remap: TM1_CH3N |
| PE13 | 66 | 44 | - | I/O | 5VT | Default: PE13 Alternate: EXMC_D10 Remap: TM1_CH3 |
| PE14 | 67 | 45 | - | I/O | 5VT | Default: PE14 Alternate: EXMC_D11 Remap: TM1_CH4 |
| PE15 | 68 | 46 | - | I/O | 5VT | Default: PE15 Alternate: EXMC_D12 Remap: TM1_BKIN |
| PB10 | 69 | 47 | 29 | I/O | 5VT | Default: PB10 Alternate: I2C2_SCL, USART3_TX, ETH_MII_RX_ER Remap: TM2_CH3 |
| PB11 | 70 | 48 | 30 | I/O | 5VT | Default: PB11 Alternate: I2C2_SDA, USART3_RX, ETH_MII_TX_EN, ETH_RMII_TX_EN Remap: TM2_CH4 |
| V _{SS_1} | 71 | 49 | 31 | P | | Default: V _{SS_1} |
| V _{DD_1} | 72 | 50 | 32 | P | | Default: V _{DD_1} |
| PB12 | 73 | 51 | 33 | I/O | 5VT | Default: PB12 Alternate: SPI2_NSS, I2C2_SMBAI, USART3_CK, TM1_BKIN, I2S2_WS ⁽³⁾ , CAN2_RX ⁽³⁾ , ETH_MII_TXD0, ETH_RMII_TXD0 |
| PB13 | 74 | 52 | 34 | I/O | 5VT | Default: PB13 Alternate: SPI2_SCK, USART3_CTS, TM1_CH1N, I2S2_CK ⁽³⁾ , CAN2_TX ⁽³⁾ , ETH_MII_TXD1, ETH_RMII_TXD1 |
| PB14 | 75 | 53 | 35 | I/O | 5VT | Default: PB14 Alternate: SPI2_MISO, USART3_RTS, TM1_CH2N, TM12_CH1 ⁽⁴⁾ |
| PB15 | 76 | 54 | 36 | I/O | 5VT | Default: PB15 Alternate: SPI2_MOSI, TM1_CH3N, I2S2_SD ⁽³⁾ , TM12_CH2 ⁽⁴⁾ |
| PD8 | 77 | 55 | - | I/O | 5VT | Default: PD8 |

| Pin Name | Pins | | | Pin Type ⁽¹⁾ | I/O ⁽²⁾ Level | Functions description |
|-------------------|---------|---------|--------|-------------------------|--------------------------|---|
| | LQFP144 | LQFP100 | LQFP64 | | | |
| | | | | | | Alternate: EXMC_D13 Remap: USART3_TX, ETH_MII_RX_DV, ETH_RMII_CRD_DV |
| PD9 | 78 | 56 | - | I/O | 5VT | Default: PD9 Alternate: EXMC_D14 Remap: USART3_RX, ETH_MII_RXD0, ETH_RMII_RXD0 |
| PD10 | 79 | 57 | - | I/O | 5VT | Default: PD10 Alternate: EXMC_D15 Remap: USART3_CK, ETH_MII_RXD1, ETH_RMII_RXD1 |
| PD11 | 80 | 58 | - | I/O | 5VT | Default: PD11 Alternate: EXMC_A16 Remap: USART3_CTS, ETH_MII_RXD2 |
| PD12 | 81 | 59 | - | I/O | 5VT | Default: PD12 Alternate: EXMC_A17 Remap: TM4_CH1, USART3_RTS |
| PD13 | 82 | 60 | - | I/O | 5VT | Default: PD13 Alternate: EXMC_A18 Remap: TM4_CH2, USART3_RTS, ETH_MII_RXD3 |
| V _{SS_8} | 83 | - | - | P | | Default: V _{SS_8} |
| V _{DD_8} | 84 | - | - | P | | Default: V _{DD_8} |
| PD14 | 85 | 61 | - | I/O | 5VT | Default: PD14 Alternate: EXMC_D0 Remap: TM4_CH3 |
| PD15 | 86 | 62 | - | I/O | 5VT | Default: PD15 Alternate: EXMC_D1 Remap: TM4_CH4 |
| PG2 | 87 | - | - | I/O | 5VT | Default: PG2 ⁽³⁾ Alternate: EXMC_A12 ⁽³⁾ |
| PG3 | 88 | - | - | I/O | 5VT | Default: PG3 ⁽³⁾ Alternate: EXMC_A13 ⁽³⁾ |
| PG4 | 89 | - | - | I/O | 5VT | Default: PG4 ⁽³⁾ Alternate: EXMC_A14 ⁽³⁾ |
| PG5 | 90 | - | - | I/O | 5VT | Default: PG5 ⁽³⁾ Alternate: EXMC_A15 ⁽³⁾ |
| PG6 | 91 | - | - | I/O | 5VT | Default: PG6 ⁽³⁾ Alternate: EXMC_INT2 ⁽³⁾ |
| PG7 | 92 | - | - | I/O | 5VT | Default: PG7 ⁽³⁾ Alternate: EXMC_INT3 ⁽³⁾ |
| PG8 | 93 | - | - | I/O | 5VT | Default: PG8 ⁽³⁾ |
| V _{SS_9} | 94 | - | - | P | | Default: V _{SS_9} |
| V _{DD_9} | 95 | - | - | P | | Default: V _{DD_9} |
| PC6 | 96 | 63 | 37 | I/O | 5VT | Default: PC6 Alternate: I2S2_MCK ⁽³⁾ ; TM8_CH1 ⁽³⁾ Remap: TM3_CH1 |

| Pin Name | Pins | | | Pin Type ⁽¹⁾ | I/O ⁽²⁾ Level | Functions description |
|-------------------|---------|---------|--------|-------------------------|--------------------------|--|
| | LQFP144 | LQFP100 | LQFP64 | | | |
| PC7 | 97 | 64 | 38 | I/O | 5VT | Default: PC7 Alternate: I2S3_MCK ⁽³⁾ ; TM8_CH2 ⁽³⁾ Remap: TM3_CH2 |
| PC8 | 98 | 65 | 39 | I/O | 5VT | Default: PC8 Alternate: TM8_CH3 ⁽³⁾ Remap: TM3_CH3 |
| PC9 | 99 | 66 | 40 | I/O | 5VT | Default: PC9 Alternate: TM8_CH4 ⁽³⁾ Remap: TM3_CH4 |
| PA8 | 100 | 67 | 41 | I/O | 5VT | Default: PA8 Alternate: USART1_CK, TM1_CH1, MCO |
| PA9 | 101 | 68 | 42 | I/O | 5VT | Default: PA9 Alternate: USART1_TX, TM1_CH2, OTG_FS_VBUS |
| PA10 | 102 | 69 | 43 | I/O | 5VT | Default: PA10 Alternate: USART1_RX, TM1_CH3, OTG_FS_ID |
| PA11 | 103 | 70 | 44 | I/O | 5VT | Default: PA11 Alternate: USART1_CTS, CANRX, OTG_FS_DM, TM1_CH4 |
| PA12 | 104 | 71 | 45 | I/O | 5VT | Default: PA12 Alternate: USART1_RTS, OTG_FS_DP, CAN1_TX, TM1_ETR |
| PA13 | 105 | 72 | 46 | I/O | 5VT | Default: JTMS, SWDIO Remap: PA13 |
| NC | 106 | 73 | - | | | - |
| V _{SS_2} | 107 | 74 | 47 | P | | Default: V _{SS_2} |
| V _{DD_2} | 108 | 75 | 48 | P | | Default: V _{DD_2} |
| PA14 | 109 | 76 | 49 | I/O | 5VT | Default: JTCK, SWCLK Remap: PA14 |
| PA15 | 110 | 77 | 50 | I/O | 5VT | Default: JTDI Alternate: SPI3_NSS ⁽³⁾ , I2S3_WS ⁽³⁾ Remap: TM2_CH1_ETR, PA15, SPI1_NSS |
| PC10 | 111 | 78 | 51 | I/O | 5VT | Default: PC10 Alternate: UART4_TX ⁽³⁾ Remap: USART3_TX, SPI3_SCK ⁽³⁾ , I2S3_CK ⁽³⁾ |
| PC11 | 112 | 79 | 52 | I/O | 5VT | Default: PC11 Alternate: UART4_RX ⁽³⁾ Remap: USART3_RX, SPI3_MISO ⁽³⁾ |
| PC12 | 113 | 80 | 53 | I/O | 5VT | Default: PC12 Alternate: UART5_TX ⁽³⁾ Remap: USART3_CK, SPI3_MOSI ⁽³⁾ , I2S3_SD ⁽³⁾ |
| PD0 | 114 | 81 | 5 | I/O | 5VT | Default: PD0 Alternate: EXMC_D2 Remap: CAN1_RX, OSC_IN |
| PD1 | 115 | 82 | 6 | I/O | 5VT | Default: PD1 Alternate: EXMC_D3 |

| Pin Name | Pins | | | Pin Type ⁽¹⁾ | I/O ⁽²⁾ Level | Functions description |
|--------------------|---------|---------|--------|-------------------------|--------------------------|---|
| | LQFP144 | LQFP100 | LQFP64 | | | |
| | | | | | | Remap: CAN1_TX, OSC_OUT |
| PD2 | 116 | 83 | 54 | I/O | 5VT | Default: PD2 Alternate: TM3_ETR, UART5_RX ⁽³⁾ |
| PD3 | 117 | 84 | - | I/O | 5VT | Default: PD3 Alternate: EXMC_CLK Remap: USART2_CTS |
| PD4 | 118 | 85 | - | I/O | 5VT | Default: PD4 Alternate: EXMC_NOE Remap: USART2_RTS |
| PD5 | 119 | 86 | - | I/O | 5VT | Default: PD5 Alternate: EXMC_NWE Remap: USART2_TX |
| V _{SS_10} | 120 | - | - | | | Default: V _{SS_10} |
| V _{DD_10} | 121 | - | - | | | Default: V _{DD_10} |
| PD6 | 122 | 87 | - | I/O | 5VT | Default: PD6 Alternate: EXMC_NWAIT Remap: USART2_RX |
| PD7 | 123 | 88 | - | I/O | 5VT | Default: PD7 Alternate: EXMC_NE1/EXMC_NCE2 Remap: USART2_CK |
| PG9 | 124 | - | - | I/O | 5VT | Default: PG9 ⁽³⁾ Alternate: EXMC_NE2 ⁽³⁾ , EXMC_NCE3 ⁽³⁾ |
| PG10 | 125 | - | - | I/O | 5VT | Default: PG10 ⁽³⁾ Alternate: EXMC_NCE4_1 ⁽³⁾ , EXMC_NE3 ⁽³⁾ |
| PG11 | 126 | - | - | I/O | 5VT | Default: PG11 ⁽³⁾ Alternate: EXMC_NCE4_2 ⁽³⁾ |
| PG12 | 127 | - | - | I/O | 5VT | Default: PG12 ⁽³⁾ Alternate: EXMC_NE4 ⁽³⁾ |
| PG13 | 128 | - | - | I/O | 5VT | Default: PG13 ⁽³⁾ Alternate: EXMC_A24 ⁽³⁾ |
| PG14 | 129 | - | - | I/O | 5VT | Default: PG14 ⁽³⁾ Alternate: EXMC_A25 ⁽³⁾ |
| V _{SS_11} | 130 | - | - | P | | Default: V _{SS_10} |
| V _{DD_11} | 131 | - | - | P | | Default: V _{DD_10} |
| PG15 | 132 | - | - | I/O | 5VT | Default: PG15 |
| PB3 | 133 | 89 | 55 | I/O | 5VT | Default: JTDO Alternate: SPI3_SCK ⁽³⁾ , I2S3_CK ⁽³⁾ Remap: PB3, TRACESWO, TM2_CH2, SPI1_SCK |
| PB4 | 134 | 90 | 56 | I/O | 5VT | Default: NJTRST Alternate: SPI3_MISO ⁽³⁾ Remap: TM3_CH1, PB4, SPI1_MISO |
| PB5 | 135 | 91 | 57 | I/O | | Default: PB5 Alternate: I2C1_SMBAL, SPI3_MOSI ⁽³⁾ , I2S3_SD ⁽³⁾ , ETH_MII_PPS, |

| Pin Name | Pins | | | Pin Type ⁽¹⁾ | I/O ⁽²⁾ Level | Functions description |
|-------------------|---------|---------|--------|-------------------------|--------------------------|--|
| | LQFP144 | LQFP100 | LQFP64 | | | |
| | | | | | | ETH_RMII_PPS_OUT Remap: TM3_CH2, SPI1_MOSI, CAN2_RX ⁽³⁾ |
| PB6 | 136 | 92 | 58 | I/O | 5VT | Default: PB6 Alternate: I2C1_SCL, TM4_CH1, Remap: USART1_TX, CAN2_TX ⁽³⁾ |
| PB7 | 137 | 93 | 59 | I/O | 5VT | Default: PB7 Alternate: I2C1_SDA, TM4_CH2, EXMC_NADV ⁽³⁾ Remap: USART1_RX |
| BOOT0 | 138 | 94 | 60 | I | | Default: BOOT0 |
| PB8 | 139 | 95 | 61 | I/O | 5VT | Default: PB8 Alternate: TM4_CH3, TM10_CH1 ⁽⁴⁾ , ETH_MII_TXD3 Remap: I2C1_SCL, CAN1_RX |
| PB9 | 140 | 96 | 62 | I/O | 5VT | Default: PB9 Alternate: TM4_CH4, TM11_CH1 ⁽⁴⁾ Remap: I2C1_SDA, CAN1_TX |
| PE0 | 141 | 97 | - | I/O | 5VT | Default: PE0 Alternate: TM4_ETR, EXMC_NBL0 |
| PE1 | 142 | 98 | - | I/O | 5VT | Default: PE1 Alternate: EXMC_NBL1 |
| V _{SS_3} | 143 | 99 | 63 | P | | Default: V _{SS_3} |
| V _{DD_3} | 144 | 100 | 64 | P | | Default: V _{DD_3} |

Notes:

1. Type: I = input, O = output, P = power.
2. I/O Level: 5VT = 5 V tolerant.
3. Functions are available in GD32F107xC, GD32F107xD, GD32F107xE, GD32F107xF, GD32F107xG devices.
4. Functions are available in GD32F107xF, GD32F107xG devices.

3 Functional description

3.1 ARM[®] Cortex[™]-M3 core

The Cortex[™]-M3 processor is the latest generation of ARM[®] processors for embedded systems. It has been developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced system response to interrupts.

- 32-bit ARM[®] Cortex[™]-M3 processor core
- Up to 108 MHz operation frequency
- Single-cycle multiplication and hardware divider
- Integrated Nested Vectored Interrupt Controller (NVIC)
- 24-bit SysTick timer

The Cortex[™]-M3 processor is based on the ARMv7 architecture and supports both Thumb and Thumb-2 instruction sets. Some system peripherals listed below are also provided by Cortex[™]-M3:

- Internal Bus Matrix connected with ICode bus, DCode bus, system bus, Private Peripheral Bus (PPB) and debug accesses (AHB-AP)
- Nested Vectored Interrupt Controller (NVIC)
- Flash Patch and Breakpoint (FPB)
- Data Watchpoint and Trace (DWT)
- Instrument Trace Macrocell (ITM)
- Memory Protection Unit (MPU)
- Serial Wire JTAG Debug Port (SWJ-DP)
- Trace Port Interface Unit (TPIU)

3.2 On-chip memory

- Up to 1024 Kbytes of Flash memory
- 96 Kbytes of SRAM

The ARM[®] Cortex[™]-M3 processor is structured in Harvard architecture which can use separate buses to fetch instructions and load/store data. 1024 Kbytes of inner Flash at most and 96 Kbytes of inner SRAM is available for storing programs and data, both accessed (R/W) at CPU clock speed with zero wait states. The Figure 6. GD32F107xx memory map shows the memory map of the GD32F107xx series of devices, including code, SRAM, peripheral, and other pre-defined regions.

3.3 Clock, reset and supply management

- Internal 8 MHz factory-trimmed RC and external 4 to 16 MHz crystal oscillator
- Internal 40 KHz RC calibrated oscillator and external 32.768 KHz crystal oscillator
- Integrated system clock PLL
- 2.6 to 3.6 V application supply and I/Os
- Supply Supervisor: POR (Power On Reset), PDR (Power Down Reset), and low voltage detector (LVD)

The Clock Control Unit (CCU) provides a range of oscillator and clock functions. These include speed internal RC oscillator and external crystal oscillator, high speed and low speed two types. Several prescalers allow the configuration of the AHB frequency, the high-speed APB (APB2) and the low-speed APB (APB1) domains. The maximum frequency of the AHB and the high-speed APB domains is 108 MHz. The maximum allowed frequency of the low-speed APB domain is 54 MHz. See Figure 7 for details on the clock tree.

The Reset Control Unit (RCU) controls three kinds of reset: system reset resets the processor core and peripheral IP components. Power-on reset (POR) and power-down reset (PDR) are always active, and ensures proper operation starting from/down to 2.6 V. The device remains in reset mode when V_{DD} is below a specified threshold. The embedded low voltage detector (LVD) monitors the power supply, compares it to the voltage threshold and generates an interrupt as a warning message for leading the MCU into security.

Power supply schemes:

- V_{DD} range: 2.6 to 3.6 V, external power supply for I/Os and the internal regulator. Provided externally through V_{DD} pins.
- V_{SSA} , V_{DDA} range: 2.6 to 3.6 V, external analog power supplies for ADC, reset blocks, RCs and PLL. V_{DDA} and V_{SSA} must be connected to V_{DD} and V_{SS} , respectively.
- V_{BAT} range: 1.8 to 3.6 V, power supply for RTC, external clock 32 kHz oscillator and backup registers (through power switch) when V_{DD} is not present.

3.4 Boot modes

At startup, boot pins are used to select one of three boot options:

- Boot from main flash memory (default)
- Boot from system memory
- Boot from on-chip SRAM

The boot loader is located in the internal boot ROM memory (system memory). It is used to reprogram the Flash memory by using USART1, USART2, CAN2, USB OTG FS in device mode. It also can be used to transfer and update the Flash memory code, the data and the vector table sections. In default condition, boot from bank 1 of Flash memory is selected. It also supports to boot from bank 2 of Flash memory by setting a bit in option bytes.

3.5 Power saving modes

The MCU supports three kinds of power saving modes to achieve even lower power consumption. They are Sleep mode, Deep-sleep mode, and Standby mode. These operating modes reduce the power consumption and allow the application to achieve the best balance between the CPU operating time, speed and power consumption.

- **Sleep mode**

In sleep mode, only the clock of CPU core is off. All peripherals continue to operate and any interrupt/event can wake up the system.

- **Deep-sleep mode**

In Deep-sleep mode, all clocks in the 1.2V domain are off, and all of the high speed crystal oscillator (HSI, HSE) and PLL are disabled. Only the contents of SRAM and registers are retained. Any interrupt or wakeup event from EXTI lines can wake up the system from the Deep-sleep mode including the 16 external lines, the RTC alarm, the LVD output, and USB wakeup. When exiting the Deep-sleep mode, the HSI is selected as the system clock.

- **Standby mode**

In Standby mode, the whole 1.2V domain is power off, the LDO is shut down, and all of HSI, HSE and PLL are disabled. The contents of SRAM and registers (except Backup Registers) are lost. There are four wakeup sources for the Standby mode, including the external reset from NRST pin, the RTC alarm, the IWDG reset, and the rising edge on WKUP pin.

3.6 Analog to digital converter (ADC)

- 12-bit SAR ADC engine
- Up to 1 MSPS conversion rate
- Conversion range: V_{SSA} to V_{DDA} (2.6 to 3.6 V)
- Temperature sensor

Up to three 12-bit 1 μ s multi-channel ADCs are integrated in the device. Each is a total of up to 21 multiplexed external channels. An analog watchdog block can be used to detect the channels, which are required to remain within a specific threshold window. A configurable channel management block of analog inputs also can be used to perform conversions in single, continuous, scan or discontinuous mode to support more advanced usages.

The ADCs can be triggered from the events generated by the general-purpose timers (TMx) and the advanced-control timers (TM1 and TM8) with internal connection. The temperature sensor has to generate a voltage that varies linearly with temperature. The conversion range is between $2.6\text{ V} < V_{DDA} < 3.6\text{ V}$. The temperature sensor is internally connected to the ADC_IN16 input channel which is used to convert the sensor output voltage into a digital value.

3.7 Digital to analog converter (DAC)

- Two 12-bit DAC converters of independent output channel
- 8-bit or 12-bit mode in conjunction with the DMA controller

The two 12-bit buffered DAC channels are used to generate variable analog outputs. The DACs are designed with integrated resistor strings structure. The DAC channels can be triggered by the timer update outputs or EXTI with DMA support. In dual DAC channel operation, conversions could be done independently or simultaneously. The maximum output value of the DAC is V_{REF+} .

3.8 DMA

- 7 channel DMA 1 controller and 5 channel DMA 2 controller
- Peripherals supported: Timers, ADC, SPIs, I²Cs, USARTs, DAC, I²S
- Dedicated DMA controller with the Ethernet application

The flexible general-purpose DMA controllers provide a hardware method of transferring data between peripherals and/or memory without intervention from the CPU, thereby freeing up bandwidth for other system functions. Four types of access method are supported: peripheral to peripheral, peripheral to memory, memory to peripheral, memory to memory

Each channel is connected to fixed hardware DMA requests. The priorities of DMA channel requests are determined by software configuration and hardware channel number. Transfer size of source and destination are independent and configurable.

3.9 General-purpose inputs/outputs (GPIOs)

- Up to 112 fast GPIOs, all mappable on 16 external interrupt vectors (EXTI)
- Analog input/output configurable
- Alternate function input/output configurable

There are up to 112 general purpose I/O pins (GPIO) in GD32F107xx, named PA0 ~ PA15 and PB0 ~ PB15, PC0 ~ PC15, PD0 ~ PD15, PE0 ~ PE15, PF0-PF15, PG0-PG15 to implement logic input/output functions. Each of the GPIO ports has related control and configuration registers to satisfy the requirements of specific applications. The external interrupts on the GPIO pins of the device have related control and configuration registers in the External Interrupt Control Unit (EXTI). The GPIO ports are pin-shared with other alternative functions (AFs) to obtain maximum flexibility on the package pins. Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions. All GPIOs are high-current capable except for analog inputs.

3.10 Timers and PWM generation

- Up to two 16-bit advanced-control timer (TM1 & TM8), ten 16-bit general-purpose timers (GPTM), and two 16-bit basic timer (TM6 & TM7)
- Up to 4 independent channels of PWM, output compare or input capture for each GPTM and external trigger input
- 16-bit, motor control PWM advanced-control timer with programmable dead-time generation for output match
- Encoder interface controller with two inputs using quadrature decoder
- 24-bit SysTick timer down counter
- 2 watchdog timers (Independent watchdog and window watchdog)

The advanced-control timer (TM1 & TM8) can be seen as a three-phase PWM multiplexed on 6 channels. It has complementary PWM outputs with programmable dead-time generation. It can also be used as a complete general-purpose timer. The 4 independent channels can be used for

- Input capture
- Output compare
- PWM generation (edge- or center-aligned counting modes)
- Single pulse mode output

If configured as a general-purpose 16-bit timer, it has the same functions as the TMx timer. It can be synchronized with external signals or to interconnect with other GPTMs together which have the same architecture and features.

The general-purpose timer (GPTM), known as TM2 ~ TM5, TM9 ~ TM11, TM12 ~ TM14 can be used for a variety of purposes including general time, input signal pulse width measurement or output waveform generation such as a single pulse generation or PWM output, up to 4 independent channels for input capture/output compare. The GPTM also supports an encoder interface with two inputs using quadrature decoder.

The basic timer, known as TM6 and TM7 are mainly used for DAC trigger generation. They can also be used as a simple 16-bit time base.

The GD32F107xx have two watchdog peripherals, Independent watchdog and window watchdog. They offer a combination of high safety level, flexibility of use and timing accuracy.

The independent watchdog timer includes a 12-bit down-counting counter and a 8-bit prescaler, It is clocked from an independent 40 kHz internal RC and as it operates independently of the main clock, it can operate in stop and standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free-running timer for application timeout management.

The window watchdog is based on a 7-bit down counter that can be set as free-running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in

debug mode.

The SysTick timer is dedicated for OS, but could also be used as a standard down counter. It features:

- A 24-bit down counter
- Auto reload capability
- Maskable system interrupt generation when the counter reaches 0
- Programmable clock source

3.11 Real time clock (RTC)

- 32-bit up-counter with a programmable 20-bit prescaler
- Alarm function
- Interrupt and wake-up event

The real time clock is an independent timer which provides a set of continuously running counters which can be used with suitable software to provide a clock calendar function, and provides an alarm interrupt and an expected interrupt. The RTC features a 32-bit programmable counter for long-term measurement using the compare register to generate an alarm. A 20-bit prescaler is used for the time base clock and is by default configured to generate a time base of 1 second from a clock at 32.768 kHz from external crystal oscillator.

3.12 Inter-integrated circuit (I2C)

- Up to two I2C bus interfaces can support both master and slave mode with a frequency up to 400 kHz
- Provide arbitration function, optional PEC (packet error checking) generation and checking
- Supports 7-bit and 10-bit addressing mode and general call addressing mode

The I2C interface is an internal circuit allowing communication with an external I2C interface which is an industry standard two line serial interface used for connection to external hardware. These two serial lines are known as a serial data line (SDA) and a serial clock line (SCL). The I2C module provides two data transfer rates: 100 kHz of standard mode or 400 kHz of the fast mode. The I2C module also has an arbitration detect function to prevent the situation where more than one master attempts to transmit data to the I2C bus at the same time. A CRC-8 calculator is also provided in I2C interface to perform packet error checking for I2C data.

3.13 Serial peripheral interface (SPI)

- Up to two SPI interfaces with a frequency of up to 18 MHz
- Support both master and slave mode
- Hardware CRC calculation and transmit automatic CRC error checking

The SPI interface uses 4 pins, among which are the serial data input and output lines (MISO & MOSI), the clock line (SCK) and the slave select line (NSS). Both SPIs can be served by the DMA controller. The SPI interface may be used for a variety of purposes, including simplex synchronous transfers on two lines with a possible bidirectional data line or reliable communication using CRC checking.

3.14 Universal synchronous asynchronous receiver transmitter (USART)

- Up to three USARTs with operating frequency up to 4.5 MHz
- Supports both asynchronous and clocked synchronous serial communication modes
- IrDA SIR encoder and decoder support
- LIN break generation and detection
- USARTs support ISO 7816-3 compliant smart card interface

The USART (USART1, USART2 and USART3) are used to translate data between parallel and serial interfaces, provides a flexible full duplex data exchange using synchronous or asynchronous transfer. It is also commonly used for RS-232 standard communication. The USART includes a programmable baud rate generator which is capable of dividing the system clock to produce a dedicated clock for the USART transmitter and receiver. The USART also supports DMA function for high speed data communication except UART5.

3.15 Inter-IC sound (I2S)

- Two I2S bus Interfaces with sampling frequency from 8 kHz to 192 kHz
- Support either master or slave mode

The Inter-IC sound (I2S) bus provides a standard communication interface for digital audio applications by 3-wire serial lines. GD32F107xx contain two I2S-bus interfaces that can be operated with 16/32 bit resolution in master or slave mode, pin multiplexed with SPI2 and SPI3. The audio sampling frequency from 8 kHz to 192 kHz is supported with less than 0.5% accuracy error.

3.16 Universal serial bus on-the-go full-speed (USB OTG FS)

- One USB device/host/OTG full-speed Interface with frequency up to 12 Mbit/s
- Internal main PLL for USB CLK compliantly

The Universal Serial Bus (USB) is a 4-wire bus with 4 bidirectional endpoints. The device controller enables 12 Mbit/s data exchange with integrated transceivers in device/host/OTG mode. Full-speed peripheral is compliant with the USB 2.0 specification. Transaction formatting is performed by the hardware, including CRC generation and checking. The status of a completed USB transfer or error condition is indicated by status registers. An interrupt is also generated if enabled. The dedicated 48 MHz clock is generated from the internal main PLL (the clock source must use a HSE crystal oscillator) and the operating frequency divided from APB1 should be 12 MHz above.

3.17 Controller area network (CAN)

- Two CAN2.0B interface with communication frequency up to 1 Mbit/s
- Internal main PLL for USB CLK compliantly

Controller area network (CAN) is a method for enabling serial communication in field bus. The CAN protocol has been used extensively in industrial automation and automotive applications. It can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers. Each CAN has three mailboxes for transmission and two FIFOs of three message deep for reception. It also provides 14 scalable/configurable identifier filter banks for selecting the incoming messages needed and discarding the others.

3.18 Ethernet MAC interface

- IEEE 802.3 compliant media access controller (MAC) for Ethernet LAN
- 10/100 Mbit/s rates with dedicated DMA controller and SRAM
- Support hardware precision time protocol (PTP) with conformity to IEEE 1588

The Ethernet media access controller (MAC) conforms to IEEE 802.3 specifications and fully supports IEEE 1588 standards. The embedded MAC provides the interface to the required external network physical interface (PHY) for LAN bus connection via an internal media independent interface (MII) or a reduced media independent interface (RMII). The number of MII signals provided up to 17 with 25 MHz output and RMII up to 9 with 50 MHz output. The function of 32-bit CRC checking is also available.

3.19 External memory controller (EXMC)

- Supported external memory: SRAM, PSRAM, ROM and NOR-Flash, NAND Flash and CF card
- Up to 16-bit data bus
- Support to interface with Motorola 6800 and Intel 8080 type LCD directly

External memory controller (EXMC) is an abbreviation of external memory controller. It is divided in to several sub-banks for external device support, each sub-bank has its own chip selection signal but at one time, only one bank can be accessed. The EXMC support code execution from external memory except NAND Flash and CF card. The EXMC also can be configured to interface with the most common LCD module of Motorola 6800 and Intel 8080 series and reduce the system cost and complexity.

3.20 Debug mode

- Serial wire JTAG debug port (SWJ-DP)

The ARM[®] SWJ-DP Interface is embedded and is a combined JTAG and serial wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target.

3.21 Package and operation temperature

- LQFP144 (GD32F107Zx), LQFP100 (GD32F107Vx), LQFP64 (GD32F107Rx)
- Operation temperature range: -40°C to +85°C (industrial level)

4 Electrical characteristics

4.1 Absolute maximum ratings

The maximum ratings are the limits to which the device can be subjected without permanently damaging the device. Note that the device is not guaranteed to operate properly at the maximum ratings. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

Table 3. Absolute maximum ratings

| Symbol | Parameter | Min | Max | Unit |
|-----------|----------------------------------|-----------------|-----------------|------|
| V_{DD} | External voltage range | $V_{SS} - 0.3$ | $V_{SS} + 3.6$ | V |
| V_{DDA} | External analog supply voltage | $V_{SSA} - 0.3$ | $V_{SSA} + 3.6$ | V |
| V_{BAT} | External battery supply voltage | $V_{SS} - 0.3$ | $V_{SS} + 3.6$ | V |
| V_{IN} | Input voltage on 5V tolerant pin | $V_{SS} - 0.3$ | $V_{SS} + 5.5$ | V |
| | Input voltage on other I/O | $V_{SS} - 0.3$ | $V_{DD} + 0.3$ | V |
| I_{IO} | Maximum current for GPIO pins | — | 25 | mA |
| T_A | Operating temperature range | -40 | +85 | °C |
| T_{STG} | Storage temperature range | -55 | +150 | °C |
| T_J | Maximum junction temperature | — | 125 | °C |

4.2 Recommended DC characteristics

Table 4. DC operating conditions

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-----------|------------------------|------------------|-----|-----|-----|------|
| V_{DD} | Supply voltage | — | 2.6 | 3.3 | 3.6 | V |
| V_{DDA} | Analog supply voltage | Same as V_{DD} | 2.6 | 3.3 | 3.6 | V |
| V_{BAT} | Battery supply voltage | — | 1.8 | — | 3.6 | V |

4.3 Power consumption

The power measurements specified in the tables represent that code with data executing from on-chip Flash with the following specifications.

Table 5. Power consumption characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|------------------|---------------------------------------|--|-----|------|-----|------|
| I _{DD} | Supply current (Run mode) | V _{DD} =V _{BAT} =3.3V, HSE=8MHz, System clock=108 MHz, All peripherals enabled | — | 45.2 | — | mA |
| | | V _{DD} =V _{BAT} =3.3V, HSE=8MHz, System clock =108 MHz, All peripherals disabled | — | 36.0 | — | mA |
| | | V _{DD} =V _{BAT} =3.3V, HSE=8MHz, System clock =72MHz, All peripherals enabled | — | 32.4 | — | mA |
| | | V _{DD} =V _{BAT} =3.3V, HSE=8MHz, System Clock =72 MHz, All peripherals disabled | — | 26.1 | — | mA |
| | Supply current (Sleep mode) | V _{DD} =V _{BAT} =3.3V, HSE=8MHz, CPU clock off, All peripherals enabled | — | 23.2 | — | mA |
| | | V _{DD} =V _{BAT} =3.3V, HSE=8MHz, CPU clock off, All peripherals disabled | — | 13.9 | — | mA |
| | Supply current (Deep-Sleep mode) | V _{DD} =V _{BAT} =3.3V, All clock off, LSI on, RTC on, All GPIOs analog mode | — | 0.65 | 1.4 | mA |
| | Supply current (Standby mode) | V _{DD} =V _{BAT} =3.3V, LDO off, LSE off, LSI on, RTC on | — | 20.5 | — | μA |
| I _{BAT} | Battery supply current (Standby mode) | V _{DD} not available, V _{BAT} =3.3V, LDO off, LSE on, LSI off, RTC on | — | 10.1 | — | μA |
| | | V _{DD} not available, V _{BAT} =3.3 V, LDO off, LSE off, LSI on, RTC on | — | 6.8 | — | μA |

4.4 EMC characteristics

EMS (electromagnetic susceptibility) includes ESD (Electrostatic discharge, positive and negative) and FTB (Burst of Fast Transient voltage, positive and negative) testing result is given in the following table, based on the EMS levels and classes compliant with IEC 61000 series standard.

Table 6. EMS characteristics

| Symbol | Parameter | Conditions | Level/Class |
|------------------|--|---|-------------|
| V _{ESD} | Voltage applied to all device pins to induce a functional disturbance | VDD = 3.3 V, TA = +25 °C conforms to IEC 61000-4-2 | 3B |
| V _{FTB} | Fast transient voltage burst applied to induce a functional disturbance through 100 pF on V _{DD} and V _{SS} pins | VDD = 3.3 V, TA = +25 °C conforms to IEC 61000-4-4 | 4A |

EMI (Electromagnetic Interference) emission testing result is given in the following table, compliant with IEC 61967-2 standard which specifies the test board and the pin loading.

Table 7. EMI characteristics

| Symbol | Parameter | Conditions | Tested frequency band | Conditions | | | Unit |
|------------------|------------|---|-----------------------|------------|------|------|------|
| | | | | 56M | 72M | 108M | |
| S _{EMI} | Peak level | VDD = 3.3 V, TA = +25 °C, compliant with IEC 61967-2 | 0.1 to 2 MHz | <0 | <0 | <0 | dBμV |
| | | | 2 to 30 MHz | -3.7 | -2.8 | -1.6 | |
| | | | 30 to 130 MHz | -6.5 | -8 | -5.5 | |
| | | | 130 MHz to 1GHz | -7 | -7 | -5 | |

4.5 Electrical sensitivity

The device is strained in order to determine its performance in terms of electrical sensitivity. Electrostatic discharges (ESD) are applied directly to the pins of the sample. Static latch-up (LU) test is based on the two measurement methods.

Table 8. ESD characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|----------------|---|---|-----|-----|------|------|
| $V_{ESD(HBM)}$ | Electrostatic discharge voltage (human body model) | $T_A=25\text{ }^\circ\text{C}$; JESD22-A114 | — | — | 4000 | V |
| $V_{ESD(CDM)}$ | Electrostatic discharge voltage (charge device model) | $T_A=25\text{ }^\circ\text{C}$; JESD22-C101 | — | — | 1000 | V |

Table 9. Static latch-up characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--------|----------------------------------|---|-----|-----|-----------|------|
| LU | I-test | $T_A=25\text{ }^\circ\text{C}$; JESD78 | — | — | ± 100 | mA |
| | V_{supply} over voltage | | — | — | 5.4 | V |

4.6 External clock characteristics

Table 10. High speed external clock (HSE) characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-------------|--|--|-----|-----|-----|---------------|
| f_{HSE} | High Speed External oscillator (HSE) frequency | $V_{DD}=3.3V$ | 4 | 8 | 16 | MHz |
| C_{HSE} | Recommended load capacitance on OSC_IN and OSC_OUT | | — | 20 | 30 | pF |
| D_{HSE} | HSE oscillator duty cycle | | 48 | 50 | 52 | % |
| I_{DDHSE} | HSE oscillator operating current | $V_{DD}=3.3V$, $T_A=25\text{ }^\circ\text{C}$ | — | 1.4 | — | μA |
| t_{SUHSE} | HSE oscillator startup time | $V_{DD}=3.3V$, $T_A=25\text{ }^\circ\text{C}$ | — | 2 | — | ms |

Table 11. Low speed external clock (LSE) characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-------------|--|-----------------------|-----|--------|------|---------------|
| f_{LSE} | Low Speed External oscillator (LSE) frequency | $V_{DD}=V_{BAT}=3.3V$ | — | 32.768 | 1000 | KHz |
| C_{LSE} | Recommended load capacitance on OSC32_IN and OSC32_OUT | | — | — | 15 | pF |
| D_{LSE} | LSE oscillator duty cycle | | 48 | 50 | 52 | % |
| I_{DDLSE} | LSE oscillator operating current | $V_{DD}=V_{BAT}=3.3V$ | — | 1.4 | — | μA |
| t_{SULSE} | LSE oscillator startup time | $V_{DD}=V_{BAT}=3.3V$ | — | 3 | — | s |

4.7 Internal clock characteristics

Table 12. High speed internal clock (HSI) characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---------------------------|--|---|-----|-----|-----|---------------|
| f_{HSI} | High Speed Internal Oscillator (HSI) frequency | $V_{\text{DD}}=3.3\text{V}$, $T_{\text{A}}=-40^{\circ}\text{C} \sim +85^{\circ}\text{C}$ | — | 8 | — | MHz |
| ACC_{HSI} | HSI oscillator Frequency accuracy | Factory-trimmed $V_{\text{DD}}=3.3\text{V}$, $T_{\text{A}}=25^{\circ}\text{C}$ | +1 | — | -1 | % |
| D_{HSI} | HSI oscillator duty cycle | $V_{\text{DD}}=3.3\text{V}$, $f_{\text{HSI}}=8\text{MHz}$ | 48 | 50 | 52 | % |
| I_{DDHSI} | HSI oscillator operating current | $V_{\text{DD}}=3.3\text{V}$, $f_{\text{HSI}}=8\text{MHz}$ | — | 80 | 100 | μA |
| t_{SUHSI} | HSI oscillator startup time | $V_{\text{DD}}=3.3\text{V}$, $f_{\text{HSI}}=8\text{MHz}$ | 1 | — | 2 | μs |

Table 13. Low speed internal clock (LSI) characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---------------------|---|---|-----|-----|-----|---------------|
| f_{LSI} | Low Speed Internal oscillator (LSI) frequency | $V_{\text{DD}}=V_{\text{BAT}}=3.3\text{V}$, $T_{\text{A}}=-40^{\circ}\text{C} \sim +85^{\circ}\text{C}$ | 30 | 40 | 60 | KHz |
| $I_{\text{DDL SI}}$ | LSI oscillator operating current | $V_{\text{DD}}=V_{\text{BAT}}=3.3\text{V}$, $T_{\text{A}}=25^{\circ}\text{C}$ | — | 1 | 2 | μA |
| t_{SULSI} | LSI oscillator startup time | $V_{\text{DD}}=V_{\text{BAT}}=3.3\text{V}$, $T_{\text{A}}=25^{\circ}\text{C}$ | — | — | 80 | μs |

4.8 PLL characteristics

Table 14. PLL characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--------------------|----------------------------|------------|-----|-----|-----|---------------|
| f_{PLLIN} | PLL input clock frequency | | 1 | 8 | 25 | MHz |
| f_{PLL} | PLL output clock frequency | | 16 | — | 108 | MHz |
| t_{LOCK} | PLL lock time | | — | | 100 | μs |

4.9 Memory characteristics

Table 15. Flash memory characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--------------------------|---|---|-----|-----|-----|---------------|
| PE_{CYC} | Number of guaranteed program /erase cycles before failure (Endurance) | $T_{\text{A}}=-40^{\circ}\text{C} \sim +85^{\circ}\text{C}$ | 100 | — | — | kcycles |
| t_{RET} | Data retention time | $T_{\text{A}}=125^{\circ}\text{C}$ | 20 | — | — | years |
| t_{PROG} | Word programming time | $T_{\text{A}}=-40^{\circ}\text{C} \sim +85^{\circ}\text{C}$ | 200 | — | 400 | μs |
| t_{ERASE} | Page erase time | $T_{\text{A}}=-40^{\circ}\text{C} \sim +85^{\circ}\text{C}$ | 60 | 100 | 450 | ms |
| t_{MERASE} | Mass erase time | $T_{\text{A}}=-40^{\circ}\text{C} \sim +85^{\circ}\text{C}$ | 3.2 | — | 9.6 | s |

4.10 GPIO characteristics

Table 16. I/O port characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|----------|-----------------------------|-----------------|------|-----|-----|------------|
| V_{IL} | Low level input voltage | $V_{DD}=2.6V$ | -0.3 | — | 0.9 | V |
| V_{IH} | High level input voltage | $V_{DD}=2.6V$ | 1 | — | 5.5 | V |
| V_{OL} | Low level output voltage | $V_{DD}=2.6V$ | — | — | 0.2 | V |
| V_{OH} | High level output voltage | $V_{DD}=2.6V$ | 2.3 | — | — | V |
| R_{PU} | Internal pull-up resistor | $V_{IN}=V_{SS}$ | 30 | 40 | 50 | k Ω |
| R_{PD} | Internal pull-down resistor | $V_{IN}=V_{DD}$ | 30 | 40 | 50 | k Ω |

4.11 ADC characteristics

Table 17. ADC characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---------------|----------------------------------|---------------------------------|-----|-----|------------|------------|
| V_{DDA} | Operating voltage | | 2.6 | 3.3 | 3.6 | V |
| V_{ADCIN} | ADC input voltage range | | 0 | — | V_{REF+} | V |
| f_{ADC} | ADC clock | | 0.6 | — | 14 | MHz |
| f_S | Sampling rate | | — | — | 1 | MHz |
| $f_{ADCCONV}$ | ADC conversion time | $f_{ADC}=14MHz$ | 1 | — | 18 | μs |
| R_{ADC} | Input sampling switch resistance | | — | — | 1 | k Ω |
| C_{ADC} | Input sampling capacitance | No pin/pad capacitance included | — | 32 | — | pF |
| t_{SU} | Startup time | | — | — | 1 | μs |

4.12 DAC characteristics

Table 18. DAC characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-------------|----------------------------------|---|-----|-----|------------|------------|
| V_{DDA} | Operating voltage | | 2.6 | 3.3 | 3.6 | V |
| V_{DACIN} | DAC input voltage range | | 0 | — | V_{REF+} | V |
| R_{LOAD} | Load resistance | Resistive load vs. V_{SSA} with buffer ON | 5 | — | — | k Ω |
| C_{LOAD} | Load capacitance | No pin/pad capacitance included | — | — | 50 | pF |
| DNE | Differential non-linearity error | DAC in 12-bit | — | — | ± 3 | LSB |
| INL | Integral non-linearity | DAC in 12-bit | — | — | ± 4 | LSB |
| Offset | Offset error | DAC in 12-bit, $V_{REF+} = 3.6 V$ | — | — | ± 12 | LSB |
| GE | Gain error | DAC in 12-bit | — | — | ± 0.5 | % |

4.13 I2C characteristics

Table 19. I2C characteristics

| Symbol | Parameter | Conditions | Standard mode | | Fast mode | | Unit |
|--------------|---------------------|------------|---------------|-----|-----------|-----|------|
| | | | Min | Max | Min | Max | |
| f_{SCL} | SCL clock frequency | | 0 | 100 | 0 | 400 | KHz |
| $t_{SCL(H)}$ | SCL clock high time | | 4.0 | — | 0.6 | — | ns |
| $t_{SCL(L)}$ | SCL clock low time | | 4.7 | — | 1.3 | — | ns |

4.14 SPI characteristics

Table 20. SPI characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|------------------------|--------------------------|------------------|-----|-----|-----|------|
| f_{SCK} | SCK clock frequency | | — | — | 18 | MHz |
| $t_{SCK(H)}$ | SCK clock high time | | 19 | — | — | ns |
| $t_{SCK(L)}$ | SCK clock low time | | 19 | — | — | ns |
| SPI master mode | | | | | | |
| $t_{V(MO)}$ | Data output valid time | | — | — | 25 | ns |
| $t_{H(MO)}$ | Data output hold time | | 2 | — | — | ns |
| $t_{SU(MI)}$ | Data input setup time | | 5 | — | — | ns |
| $t_{H(MI)}$ | Data input hold time | | 5 | — | — | ns |
| SPI slave mode | | | | | | |
| $t_{SU(NSS)}$ | NSS enable setup time | $f_{PCLK}=54MHz$ | 74 | — | — | ns |
| $t_{H(NSS)}$ | NSS enable hold time | $f_{PCLK}=54MHz$ | 37 | — | — | ns |
| $t_{A(SO)}$ | Data output access time | $f_{PCLK}=54MHz$ | 0 | — | 55 | ns |
| $t_{DIS(SO)}$ | Data output disable time | | 3 | — | 10 | ns |
| $t_{V(SO)}$ | Data output valid time | | — | — | 25 | ns |
| $t_{H(SO)}$ | Data output hold time | | 15 | — | — | ns |
| $t_{SU(SI)}$ | Data input setup time | | 5 | — | — | ns |
| $t_{H(SI)}$ | Data input hold time | | 4 | — | — | ns |

5 Package information

Figure 7. LQFP package outline

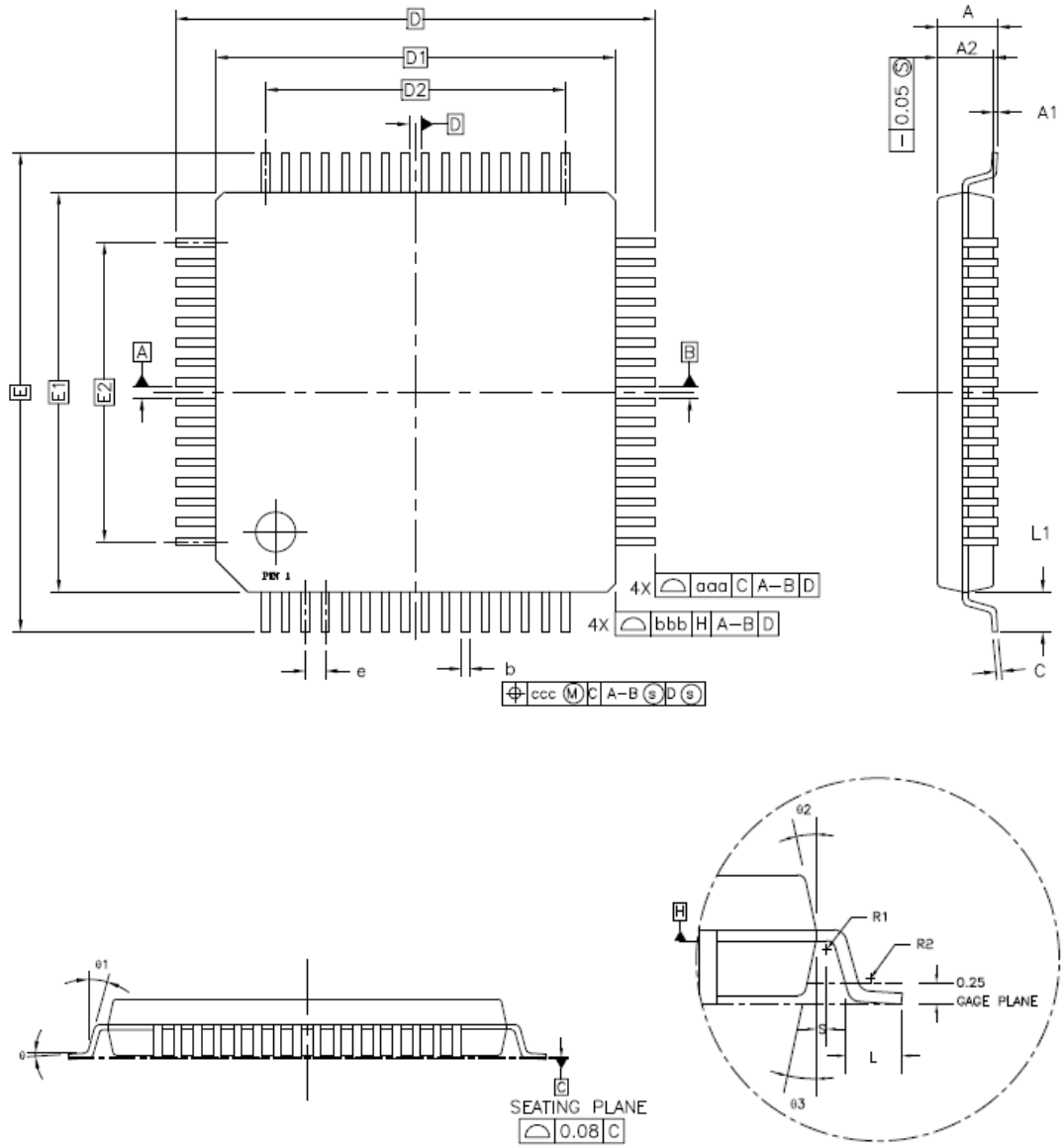


Table 21. LQFP package dimensions

| Symbol | LQFP64 | | | LQFP100 | | | LQFP144 | | |
|------------|--------|-------|------|---------|-------|------|---------|-------|------|
| | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max |
| A | - | - | 1.60 | - | - | 1.60 | - | - | 1.60 |
| A1 | 0.05 | - | 0.15 | 0.05 | - | 0.15 | 0.05 | - | 0.15 |
| A2 | 1.35 | 1.40 | 1.45 | 1.35 | 1.40 | 1.45 | 1.35 | 1.40 | 1.45 |
| D | - | 12.00 | - | - | 16.00 | - | - | 22.00 | - |
| D1 | - | 10.00 | - | - | 14.00 | - | - | 20.00 | - |
| E | - | 12.00 | - | - | 16.00 | - | - | 22.00 | - |
| E1 | - | 10.00 | - | - | 14.00 | - | - | 20.00 | - |
| R1 | 0.08 | - | - | 0.08 | - | - | 0.08 | - | - |
| R2 | 0.08 | - | 0.20 | 0.08 | - | 0.20 | 0.08 | - | 0.20 |
| θ | 0° | 3.5° | 7° | 0° | 3.5° | 7° | 0° | 3.5° | 7° |
| θ_1 | 0° | - | - | 0° | - | - | 0° | - | - |
| θ_2 | 11° | 12° | 13° | 11° | 12° | 13° | 11° | 12° | 13° |
| θ_3 | 11° | 12° | 13° | 11° | 12° | 13° | 11° | 12° | 13° |
| c | 0.09 | - | 0.20 | 0.09 | - | 0.20 | 0.09 | - | 0.20 |
| L | 0.45 | 0.60 | 0.75 | 0.45 | 0.60 | 0.75 | 0.45 | 0.60 | 0.75 |
| L1 | - | 1.00 | - | - | 1.00 | - | - | 1.00 | - |
| S | 0.20 | - | - | 0.20 | - | - | 0.20 | - | - |
| b | 0.17 | 0.20 | 0.27 | 0.17 | 0.20 | 0.27 | 0.17 | 0.20 | 0.27 |
| e | - | 0.50 | - | - | 0.50 | - | - | 0.50 | - |
| D2 | - | 17.50 | - | - | 7.50 | - | - | 17.50 | - |
| E2 | - | 17.50 | - | - | 7.50 | - | - | 17.50 | - |
| aaa | 0.20 | | | 0.20 | | | 0.20 | | |
| bbb | 0.20 | | | 0.20 | | | 0.20 | | |
| ccc | 0.08 | | | 0.08 | | | 0.08 | | |

(Original dimensions are in millimeters)

6 Ordering Information

Table 22. Part ordering code for GD32F107xx devices

| Ordering code | Flash (KB) | Package | Package type | Temperature operating range |
|---------------|------------|---------|--------------|------------------------------|
| GD32F107RBT6 | 128 | LQFP64 | Green | Industrial -40°C to +85°C |
| GD32F107RCT6 | 256 | LQFP64 | Green | Industrial -40°C to +85°C |
| GD32F107RDT6 | 384 | LQFP64 | Green | Industrial -40°C to +85°C |
| GD32F107RET6 | 512 | LQFP64 | Green | Industrial -40°C to +85°C |
| GD32F107RFT6 | 768 | LQFP64 | Green | Industrial -40°C to +85°C |
| GD32F107RGT6 | 1024 | LQFP64 | Green | Industrial -40°C to +85°C |
| GD32F107VBT6 | 128 | LQFP100 | Green | Industrial -40°C to +85°C |
| GD32F107VCT6 | 256 | LQFP100 | Green | Industrial -40°C to +85°C |
| GD32F107VDT6 | 384 | LQFP100 | Green | Industrial -40°C to +85°C |
| GD32F107VET6 | 512 | LQFP100 | Green | Industrial -40°C to +85°C |
| GD32F107VFT6 | 768 | LQFP100 | Green | Industrial -40°C to +85°C |
| GD32F107VGT6 | 1024 | LQFP100 | Green | Industrial -40°C to +85°C |
| GD32F107ZCT6 | 256 | LQFP144 | Green | Industrial -40°C to +85°C |
| GD32F107ZDT6 | 384 | LQFP144 | Green | Industrial -40°C to +85°C |
| GD32F107ZET6 | 512 | LQFP144 | Green | Industrial -40°C to +85°C |
| GD32F107ZFT6 | 768 | LQFP144 | Green | Industrial -40°C to +85°C |
| GD32F107ZGT6 | 1024 | LQFP144 | Green | Industrial -40°C to +85°C |

7 Revision History

Table 23. Revision history

| Revision No. | Description | Date |
|--------------|-----------------|--------------|
| 1.0 | Initial Release | Oct.25, 2013 |