

PROTECTION PRODUCTS - RailClamp®
Description

RailClamp® low capacitance TVS array is designed to protect high speed data interfaces. This series has been specifically designed to protect sensitive components which are connected to data and transmission lines from overvoltage caused by electrostatic discharge (**ESD**), electrical fast transients (**EFT**), and **lightning**.

The unique design incorporates eight surge rated, low capacitance steering diodes and a TVS diode in a single package. During transient conditions, the steering diodes direct the transient to either the positive side of the power supply line or to ground. The internal TVS diode prevents over-voltage on the power line, protecting any downstream components.

The SRV05-4A is in a 6-lead SOT-23 package. The leads are finished with lead-free matte tin. Each device will protect up to four high-speed lines. They may be used to meet the ESD immunity requirements of IEC 61000-4-2. The combination of small size, low capacitance, and high surge capability makes them ideal for use in applications such as 10/100 Ethernet, USB 2.0, and video interfaces.

Features

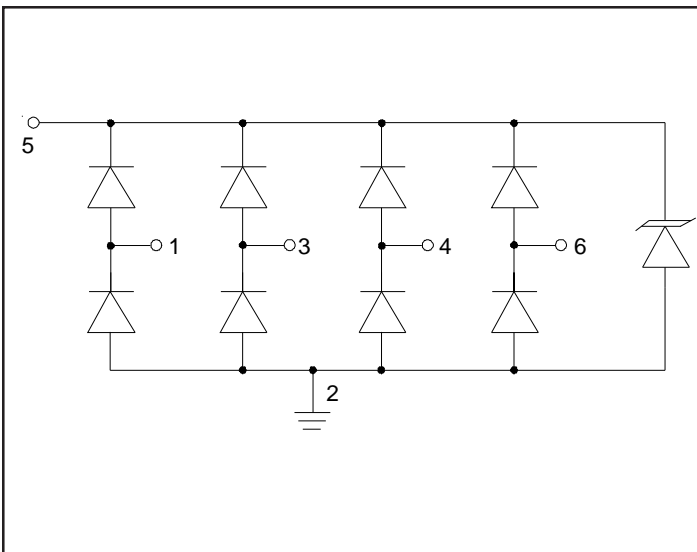
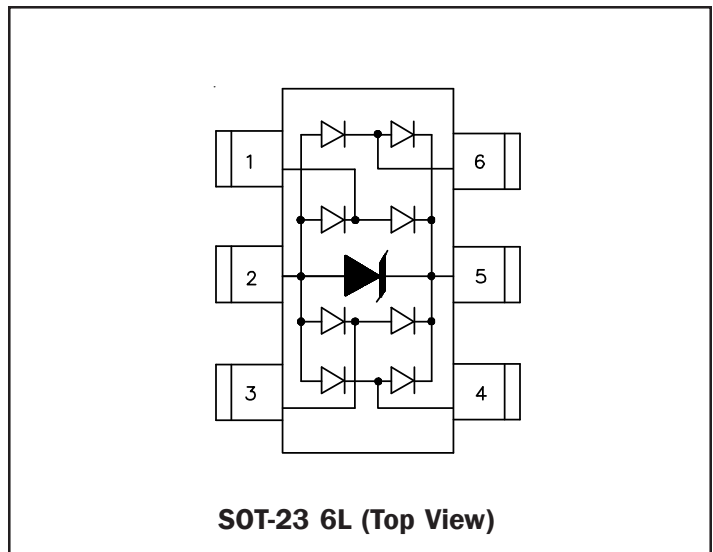
- ◆ Protection for high-speed data lines to **IEC 61000-4-2 (ESD) ±15kV (air), ±8kV (contact)**
IEC 61000-4-4 (EFT) 40A (5/50ns)
IEC 61000-4-5 (Lightning) 12A (8/20µs)
- ◆ Array of surge rated diodes with internal TVS Diode
- ◆ Small package saves board space
- ◆ Protects four I/O lines
- ◆ Low capacitance: **3pF** typical
- ◆ Low clamping voltage
- ◆ Low operating voltage: 5.0V
- ◆ Solid-state silicon-avalanche technology

Mechanical Characteristics

- ◆ JEDEC SOT-23 6L package
- ◆ Pb-Free, Halogen Free, RoHS/WEEE Compliant
- ◆ Molding compound flammability rating: UL 94V-0
- ◆ Marking: V05 + Date Code
- ◆ Packaging: Tape and Reel

Applications

- ◆ USB 2.0 Power and Data Line Protection
- ◆ Video Graphics Cards
- ◆ Monitors and Flat Panel Displays
- ◆ Digital Visual Interface (DVI)
- ◆ 10/100 Ethernet
- ◆ Notebook Computers
- ◆ SIM Ports
- ◆ IEEE 1394 Firewire Ports

Circuit Diagram

Schematic and PIN Configuration


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Absolute Maximum Rating

Rating	Symbol	Value	Units
Peak Pulse Power (tp = 8/20μs)	P_{pk}	300	Watts
Peak Pulse Current (tp = 8/20μs)	I_{pp}	12	A
ESD per IEC 61000-4-2 (Air) ESD per IEC 61000-4-2 (Contact)	V_{ESD}	15 8	kV
Lead Soldering Temperature	T_L	260 (10 sec.)	°C
Operating Temperature	T_J	-55 to +125	°C
Storage Temperature	T_{STG}	-55 to +150	°C

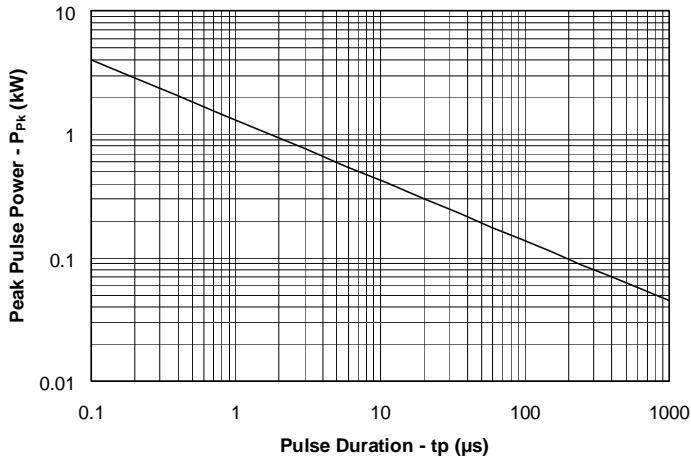
Electrical Characteristics (T=25°C)

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units
Reverse Stand-Off Voltage	V_{RWM}	Pin 5 to 2			5	V
Reverse Breakdown Voltage	V_{BR}	$I_t = 1mA$ Pin 5 to 2	6			V
Reverse Leakage Current	I_R	$V_{RWM} = 5V, T=25°C$ Pin 5 to 2			5	μA
Forward Voltage	V_F	$I_f = 15mA$			1.2	V
Clamping Voltage	V_C	$I_{pp} = 1A, tp = 8/20μs$ Any I/O pin to Ground			12.5	V
Clamping Voltage	V_C	$I_{pp} = 5A, tp = 8/20μs$ Any I/O pin to Ground			17.5	V
Junction Capacitance	C_J	$V_R = 0V, f = 1MHz$ Any I/O pin to Ground		3	5	pF
		$V_R = 0V, f = 1MHz$ Between I/O pins		1.5		pF

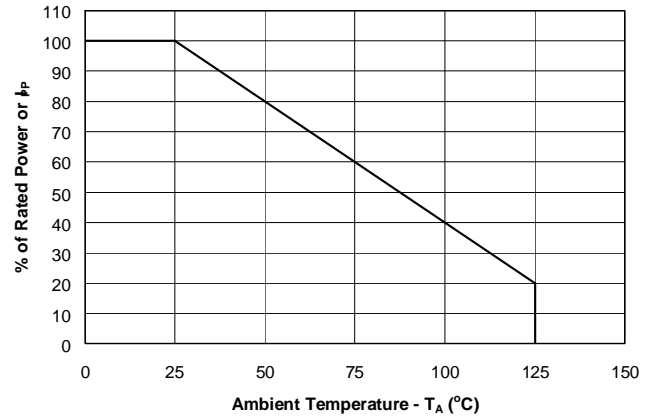
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Typical Characteristics

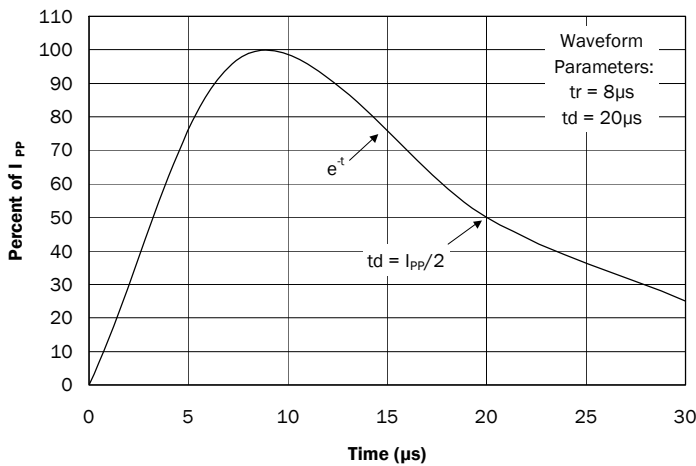
Non-Repetitive Peak Pulse Power vs. Pulse Time



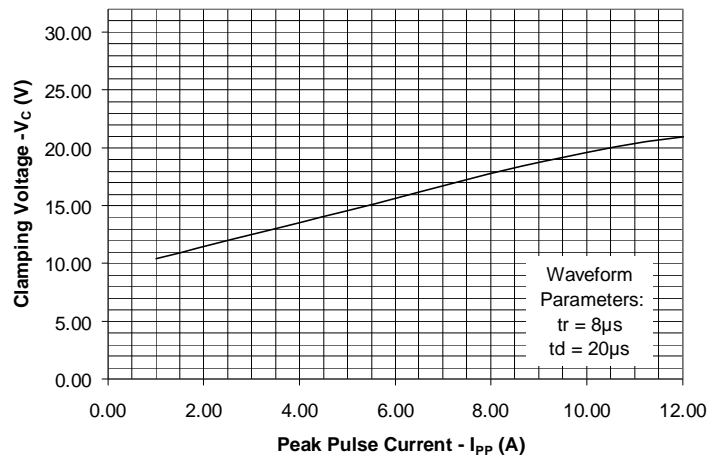
Power Derating Curve



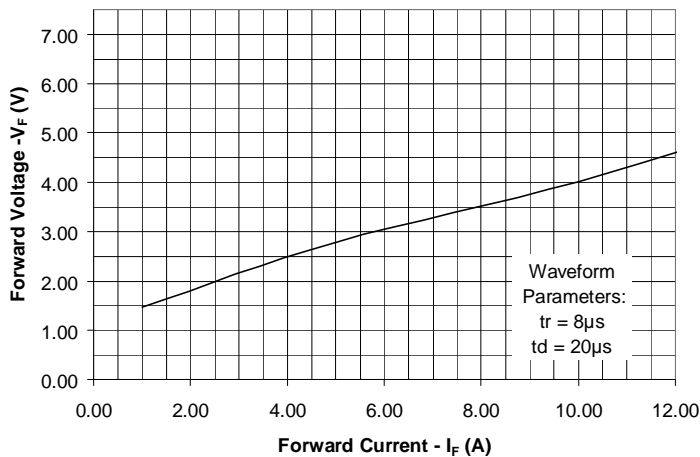
Pulse Waveform



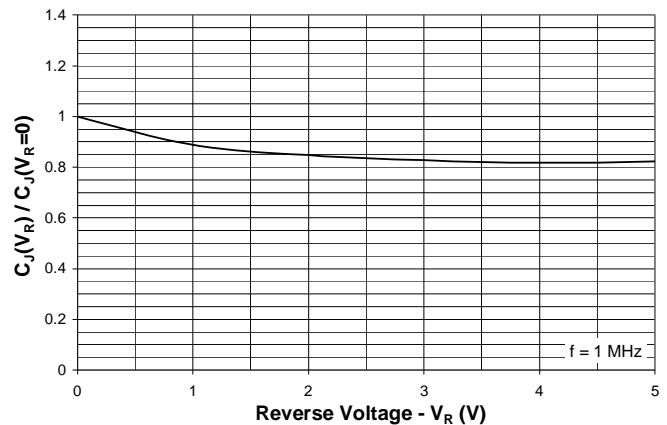
Clamping Voltage vs. Peak Pulse Current

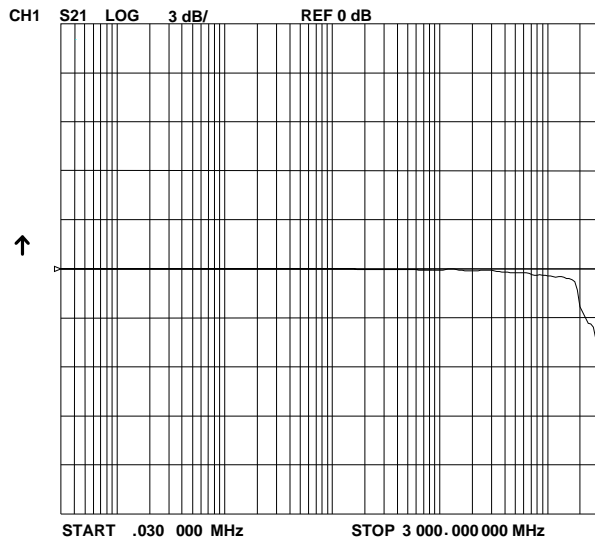
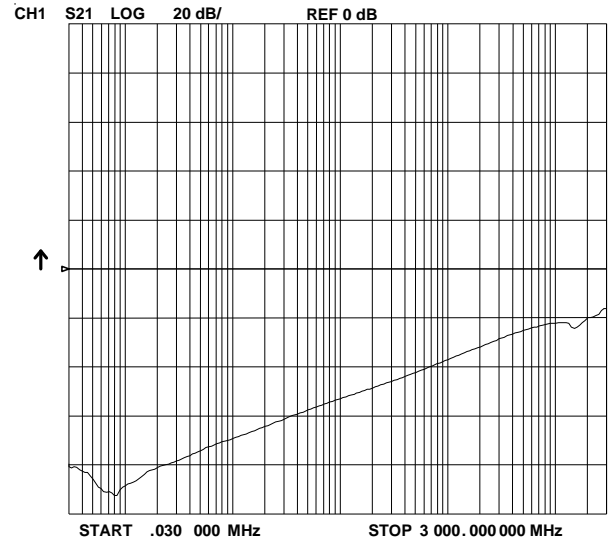


Forward Voltage vs. Forward Current



Normalized Capacitance vs. Reverse Voltage



Insertion Loss S21

Analog Cross Talk


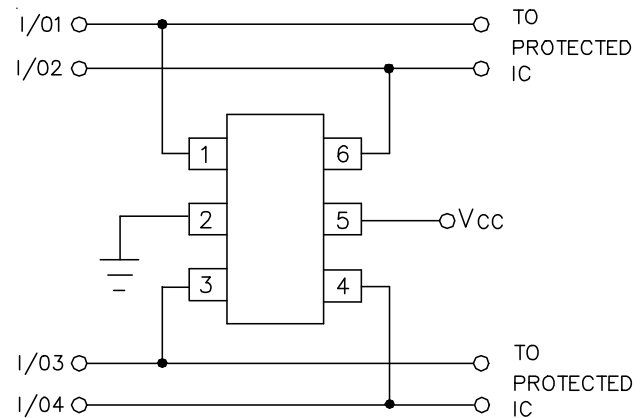
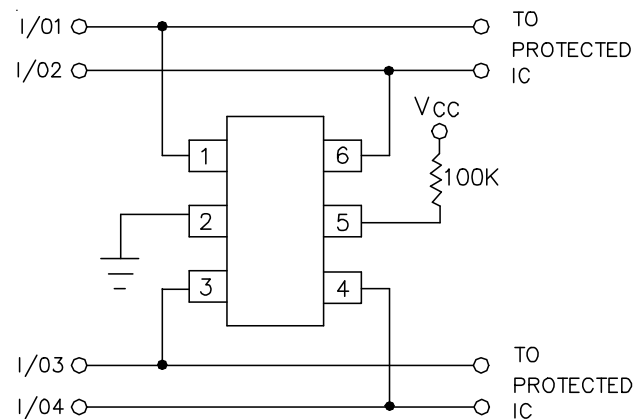
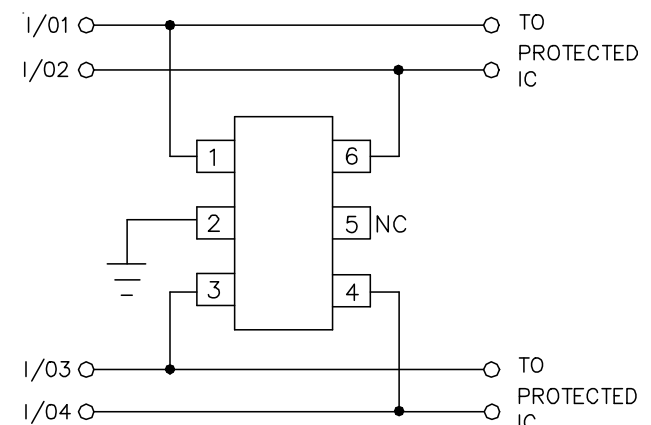
PROTECTION PRODUCTS
Applications Information
Device Connection Options for Protection of Four High-Speed Data Lines

The SRV05-4A is designed to protect four data lines from transient over-voltages by clamping them to a fixed reference. When the voltage on the protected line exceeds the reference voltage (plus diode V_F) the steering diodes are forward biased, conducting the transient current away from the sensitive circuitry. Data lines are connected at pins 1, 3, 4 and 6. The negative reference (REF1) is connected at pin 2. This pin should be connected directly to a ground plane on the board for best results. The path length is kept as short as possible to minimize parasitic inductance. The positive reference (REF2) is connected at pin 5. The options for connecting the positive reference are as follows:

1. To protect data lines and the power line, connect pin 5 directly to the positive supply rail (V_{CC}). In this configuration the data lines are referenced to the supply voltage. The internal TVS diode prevents over-voltage on the supply rail.
2. The SRV05-4A can be isolated from the power supply by adding a series resistor between pin 5 and V_{CC} . A value of 100k Ω is recommended. The internal TVS and steering diodes remain biased, providing the advantage of lower capacitance.
3. In applications where no positive supply reference is available, or complete supply isolation is desired, the internal TVS may be used as the reference. In this case, pin 5 is not connected. The steering diodes will begin to conduct when the voltage on the protected line exceeds the working voltage of the TVS (plus one diode drop).

ESD Protection With RailClamps®

RailClamps are optimized for ESD protection using the rail-to-rail topology. Along with good board layout, these devices virtually eliminate the disadvantages of using discrete components to implement this topology. Consider the situation shown in Figure 1 where discrete diodes or diode arrays are configured for rail-to-rail protection on a high speed line. During positive duration ESD events, the top diode will be forward biased when the voltage on the protected line exceeds

Data Line and Power Supply Protection Using V_{CC} as reference

Data Line Protection with Bias and Power Supply Isolation Resistor

Data Line Protection Using Internal TVS Diode as Reference


PROTECTION PRODUCTS

Applications Information (continued)

the reference voltage plus the V_F drop of the diode. For negative events, the bottom diode will be biased when the voltage exceeds the V_F of the diode. At first approximation, the clamping voltage due to the characteristics of the protection diodes is given by:

$$V_C = V_{CC} + V_F \quad (\text{for positive duration pulses})$$

$$V_C = -V_F \quad (\text{for negative duration pulses})$$

However, for fast rise time transient events, the effects of parasitic inductance must also be considered as shown in Figure 2. Therefore, the actual clamping voltage seen by the protected circuit will be:

$$V_C = V_{CC} + V_F + L_P di_{ESD}/dt \quad (\text{for positive duration pulses})$$

$$V_C = -V_F - L_G di_{ESD}/dt \quad (\text{for negative duration pulses})$$

ESD current reaches a peak amplitude of 30A in 1ns for a level 4 ESD contact discharge per IEC 61000-4-2. Therefore, the voltage overshoot due to 1nH of series inductance is:

$$V = L_P di_{ESD}/dt = 1 \times 10^{-9} (30 / 1 \times 10^{-9}) = 30V$$

Example:

Consider a $V_{CC} = 5V$, a typical V_F of 30V (at 30A) for the steering diode and a series trace inductance of 10nH. The clamping voltage seen by the protected IC for a positive 8kV (30A) ESD pulse will be:

$$V_C = 5V + 30V + (10nH \times 30V/nH) = 335V$$

This does not take into account that the ESD current is directed into the supply rail, potentially damaging any components that are attached to that rail. Also note that it is not uncommon for the V_F of discrete diodes to exceed the damage threshold of the protected IC. This is due to the relatively small junction area of typical discrete components. It is also possible that the power dissipation capability of the discrete diode will be exceeded, thus destroying the device.

The RailClamp is designed to overcome the inherent disadvantages of using discrete signal diodes for ESD suppression. The RailClamp's integrated TVS diode

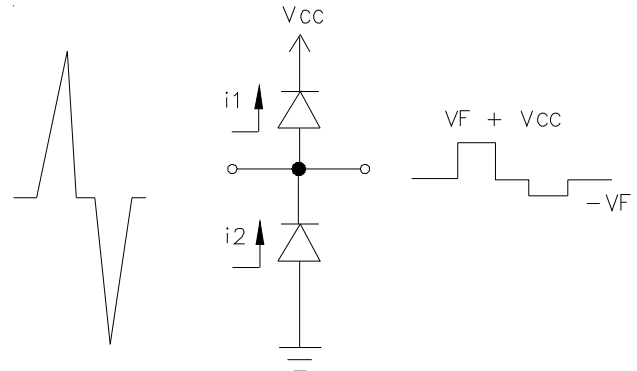


Figure 1 - "Rail-To-Rail" Protection Topology (First Approximation)

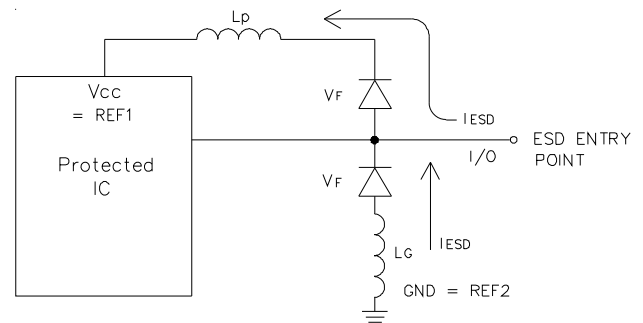


Figure 2 - The Effects of Parasitic Inductance When Using Discrete Components to Implement Rail-To-Rail Protection

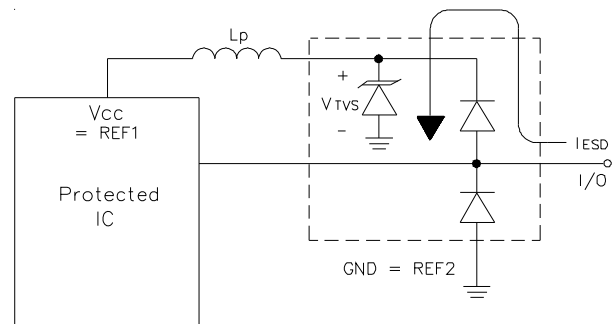


Figure 3 - Rail-To-Rail Protection Using RailClamp TVS Arrays

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Applications Information (continued)

helps to mitigate the effects of parasitic inductance in the power supply connection. During an ESD event, the current will be directed through the integrated TVS diode to ground. The maximum voltage seen by the protected IC due to this path will be the clamping voltage of the device.

Video Interface Protection

Video interfaces are susceptible to transient voltages resulting from electrostatic discharge (ESD) and “hot plugging” cables. If left unprotected, the video interface IC may be damaged or even destroyed. Protecting a high-speed video port presents some unique challenges. First, any added protection device must have extremely low capacitance and low leakage current so that the integrity of the video signal is not compromised. Second, the protection component must be able to absorb high voltage transients without damage or degradation. As a minimum, the device should be rated to handle ESD voltages per IEC 61000-4-2, level 4 ($\pm 15\text{kV}$ air, $\pm 8\text{kV}$ contact). The clamping voltage of the device (when conducting high current ESD pulses) must be sufficiently low enough to protect the sensitive CMOS IC. If the clamping voltage is too high, the “protected” device may latch-up or be destroyed. Finally, the device must take up a relatively small amount of board space, particularly in portable applications such as notebooks and handhelds. The SRV05-4A is designed to meet or exceed all of the above criteria. A typical video interface protection circuit is shown in Figure 4. All exposed lines are protected including R, G, B, H-Sync, V-Sync, and the ID lines for plug and play monitors.

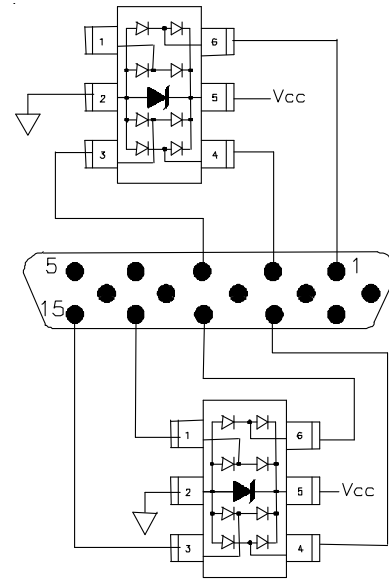


Figure 4 - Video Interface Protection

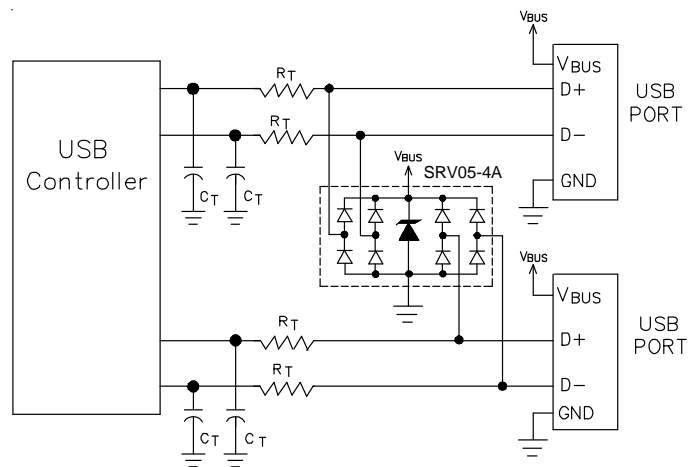


Figure 5 - Dual USB Port Protection

Universal Serial Bus ESD Protection

The SRV05-4A may also be used to protect the USB ports on monitors, computers, peripherals or portable systems. Each device will protect up to two USB ports (Figure 5). When the voltage on the data lines exceed the bus voltage (plus one diode drop), the internal rectifiers are forward biased conducting the transient current away from the protected controller chip. The TVS diode directs the surge to ground. The TVS diode also acts to suppress ESD strikes directly on the voltage bus. Thus, both power and data pins are protected with a single device.

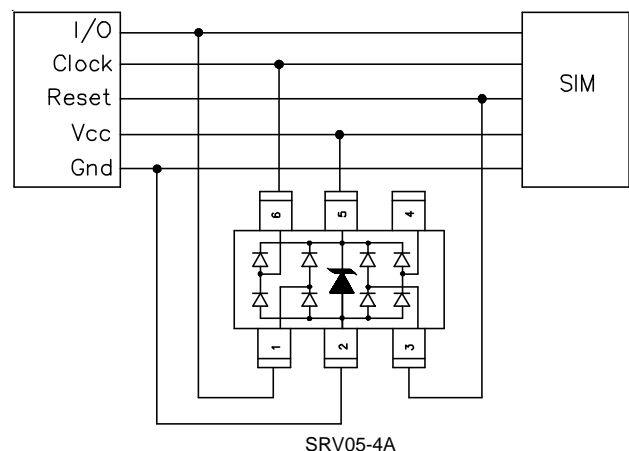


Figure 6 - SIM Port

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DVI Protection

The small geometry of a typical digital-visual interface (DVI) graphic chip will make it more susceptible to electrostatic discharges (ESD) and cable discharge events (CDE). Transient protection of a DVI port can be challenging. Digital-visual interfaces can often transmit and receive at a rate equal to or above 1Gbps. The high-speed data transmission requires the protection device to have low capacitance to maintain signal integrity and low clamping voltage to reduce stress on the protected IC. The SRV05-4A has a low typical insertion loss of <math><0.4\text{dB}</math> at 1GHz (I/O to ground) to ensure signal integrity and can protect the DVI interface to the 8kV contact and 15kV air ESD per IEC 61000-4-2 and CDE.

Figure 7 shows how to design the SRV05-4A into the DVI circuit on a flat panel display and a PC graphic card. The SRV05-4A is configured to provide common mode and differential mode protection. The internal TVS of the SRV05-4A acts as a 5 volt reference. The power pin of the DVI circuit does not come out through the connector and is not subjected to external ESD pulse; therefore, pin 5 should be left unconnected. Connecting pin 5 to Vcc of the DVI circuit may result in damage to the chip from ESD current.

10/100 ETHERNET PROTECTION

Ethernet ICs are vulnerable to damage from electrostatic discharge (ESD). The internal protection in the PHY chip, if any, often is not enough due to the high energy of the discharges specified by IEC 61000-4-2. If the discharge is catastrophic, it will destroy the protected IC. If it is less severe, it will cause latent failures that are very difficult to find.

In a typical 10/100 system, the twisted-pair interface for each port consists of two differential signal pairs: one for the transmitter and one for the receiver, with the transmitter input being the most sensitive to damage. The fatal discharge occurs differentially across the transmit or receive line pair and is capacitively coupled through the transformer to the Ethernet chip. Figure 8 shows how to design the SRV05-4A on the line side of a 10/100 ethernet port to provide differential mode protection. The common mode isolation of the transformer will provide common mode protection to the rating of the transformer isolation which is usually >1.5kV. Figure 9 shows how to implement the SRV05-4A on the IC side of the 10/100 Ethernet circuit.

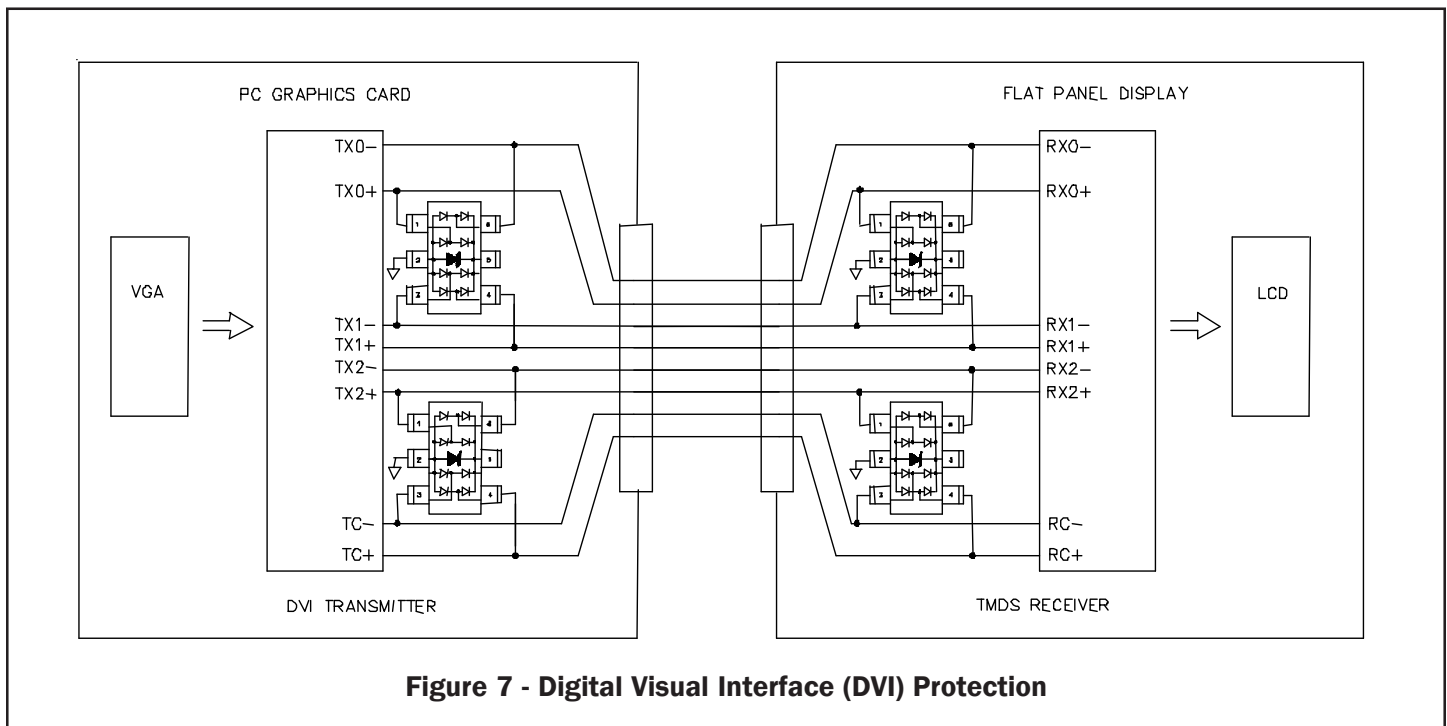


Figure 7 - Digital Visual Interface (DVI) Protection

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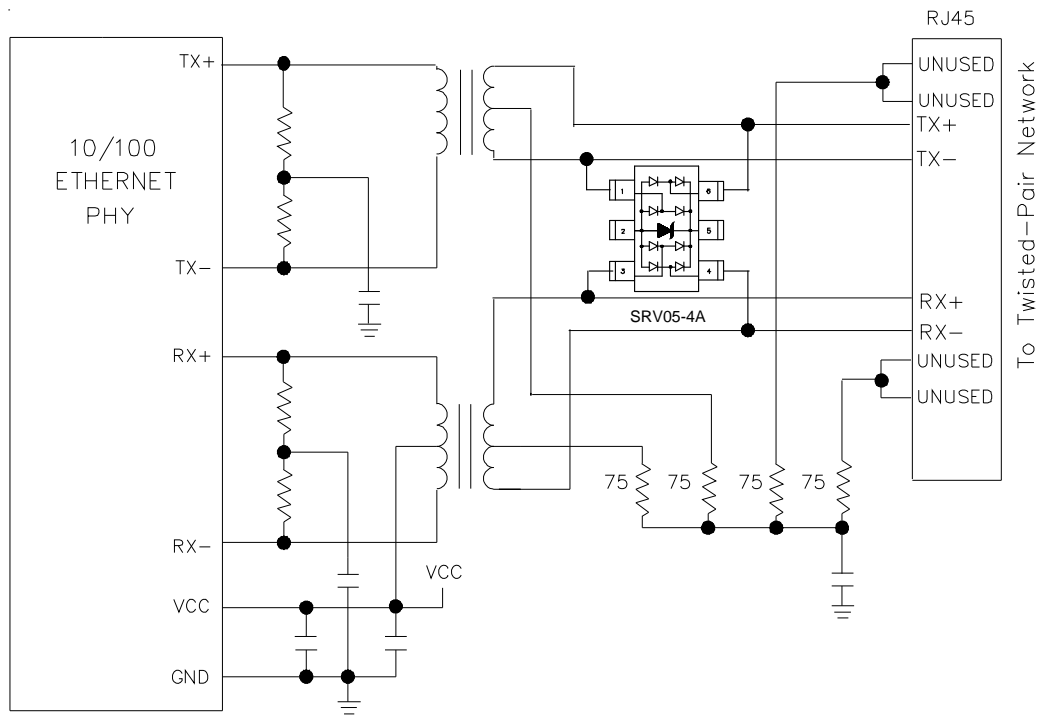


Figure 8 - 10/100 Ethernet Differential Protection

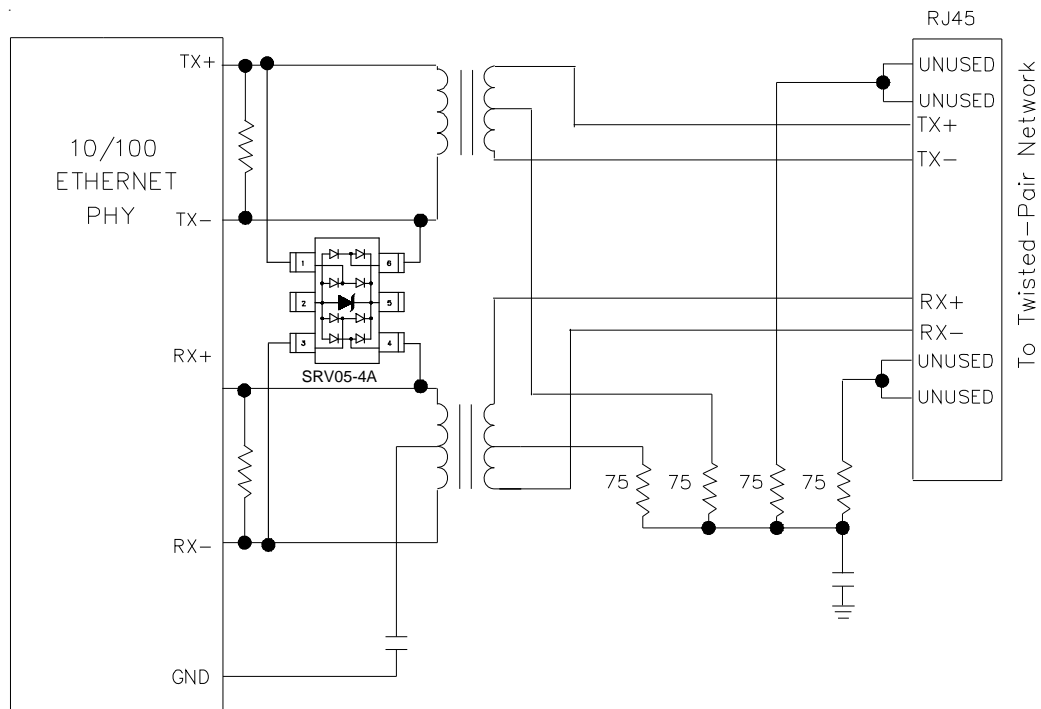
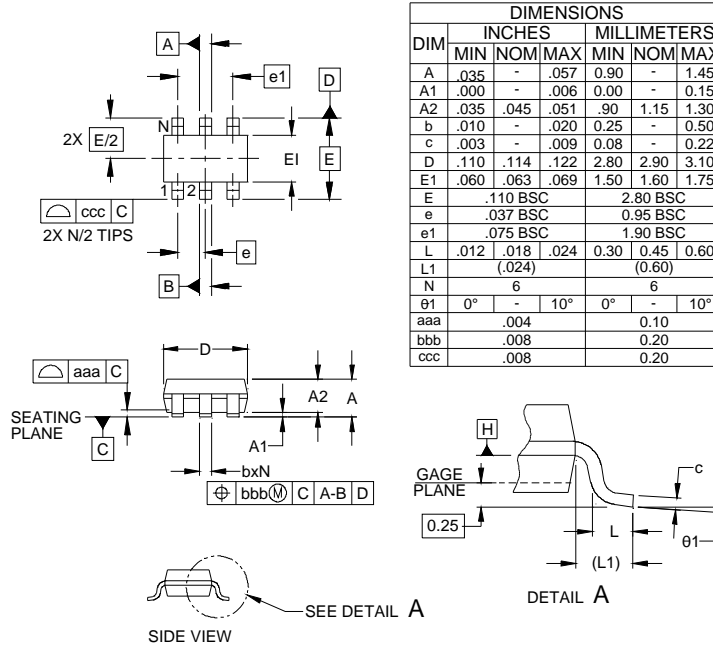


Figure 9 - 10/100 Ethernet Differential and Common Mode Protection

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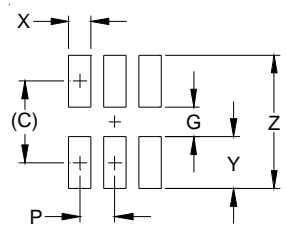
Outline Drawing -SOT23 6L



DIM	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	.035	-	.057	0.90	-	1.45
A1	.000	-	.006	0.00	-	0.15
A2	.035	.045	.051	.90	1.15	1.30
b	.010	-	.020	0.25	-	0.50
c	.003	-	.009	0.08	-	0.22
D	.110	.114	.122	2.80	2.90	3.10
E1	.060	.063	.069	1.50	1.60	1.75
E	.110 BSC			2.80 BSC		
e	.037 BSC			0.95 BSC		
e1	.075 BSC			1.90 BSC		
L	.012	.018	.024	0.30	0.45	0.60
L1	(0.024)			(0.60)		
N	6			6		
θ1	0°	-	10°	0°	-	10°
aaa	.004			0.10		
bbb	.008			0.20		
ccc	.008			0.20		

- NOTES:
1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
 2. DATUMS $\boxed{-A-}$ AND $\boxed{-B-}$ TO BE DETERMINED AT DATUM PLANE $\boxed{+H+}$
 3. DIMENSIONS "E1" AND "D" DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.

Land Pattern -SOT23 6L

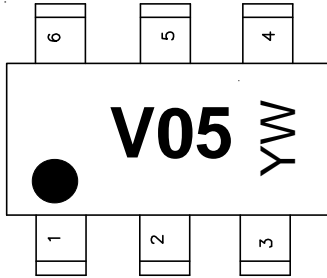


DIM	DIMENSIONS	
	INCHES	MILLIMETERS
C	(.098)	(2.50)
G	.055	1.40
P	.037	0.95
X	.024	0.60
Y	.043	1.10
Z	.141	3.60

- NOTES:
1. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.

PROTECTION PRODUCTS

Marking Codes

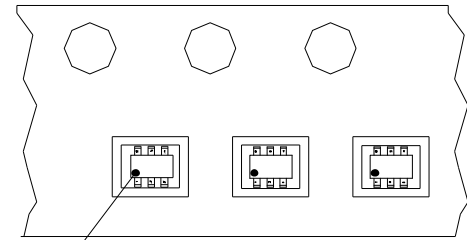
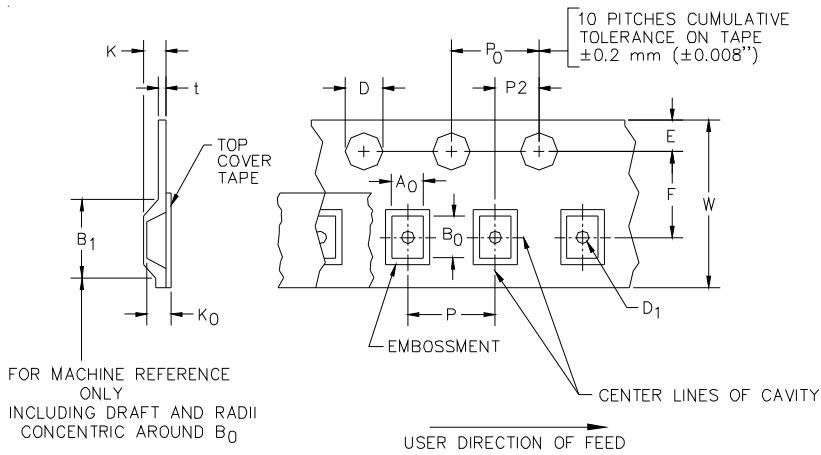


Ordering Information

Part Number	Lead Finish	Qty per Reel	Reel Size
SRV05-4ATCT	Matte Tin	3,000	7 Inch

YW = 2 - Alphanumeric characters for Date Code

Tape and Reel Specification



Pin 1 Location

→
User Direction of feed

A0	B0	K0
3.23 +/-0.05 mm	3.17 +/-0.05 mm	1.37 +/-0.05 mm

Tape Width	B, (Max)	D	D1	E	F	K (MAX)	P	P0	P2	T(MAX)	W
8 mm	4.2 mm (.165)	1.5 + 0.1 mm - 0.0 mm	1.0 mm ±0.05	1.750±.10 mm	3.5±0.05 mm	2.4 mm	4.0±0.1 mm	4.0±0.1 mm	2.0±0.05 mm	0.4 mm	8.0 mm + 0.3 mm - 0.1 mm

Contact Information

Semtech Corporation
 Protection Products Division
 200 Flynn Road, Camarillo, CA 93012
 Phone: (805)498-2111 FAX (805)498-3804

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